Characterization of negative bias temperature instability of Ge MOSFETs with GeO_2/Al_2O_3 stack

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***Abstract*—Ge is a candidate for replacing Si, especially for pMOSFETs because of its high hole mobility. For Si-pMOSFETs, negative bias temperature instabilities (NBTI) limit their lifetime. There is little information available for the NBTI of Ge-pMOSFETs with $Ge/GeO_2/Al_2O_3$ stack. The objective of this work is to provide this information and to compare the NBTI of Ge- and Si-pMOSFETs. New findings include: (i) The time exponent varies with stress biases/field when measured by either the conventional slow DC or pulse I-V technique, making the conventional Vg-accelerated method for predicting the lifetime of Si-pMOSFETs inapplicable to Ge-pMOSFETs used in this work; (ii) The NBTI is dominated by positive charges (PC) in dielectric, rather than generated interface states; (iii) The PC in $Ge/GeO_2/Al_2O_3$ can be fully annealed at 150 ^oC; and (iv) The defect losses reported for Si sample were not observed. For the first time, we report that the PCs in oxides on Ge and Si behave differently and, to explain the difference, an energy-switching model is proposed for hole traps in Ge-MOSEFTs: their energy levels have a spread below the edge of valence band, i.e. Ev, when neutral, lift well above Ev after charging, and return below Ev following neutralization.**

***Index Terms*—Ge MOSFETs, Ge/GeO_2, Al_2O_3, NBTI, High-k on Ge, Hole traps, Positive charges, Degradations, Lifetime.**

I. INTRODUCTION

The successful downscaling of Si MOSFETs has enabled a continuous increase of devices per chip and the operation speed since 1960s, but it is approaching its end since the device is running out of atoms and its leakage and variability is becoming intolerable [1-6]. To continue improving device speed, much effort has been made to replace Si by high mobility semiconductors [1-4]. Ge is a strong candidate, especially for pMOSFETs because its intrinsic hole mobility is about 4 times of that for Si.

Promising results have already been demonstrated for Ge pMOSFETs through two approaches. One is to use a Si-cap of several mono-layers [1, 2, 4]. This offers good compatibility with existing Si processes and the gate dielectric stack used is often the same as that for Si. However, the interface states are relatively high, the Si-cap increases the separation between gate and channel, and there are difficulties in making Ge nMOSFETs of good performance [7]. The other approach is preparing GeO_2/high-k stack directly on Ge [2, 3, 8-10]. By controlling the interaction of GeO_2 with Ge and suppressing the evaporation of GeO, it has been reported that the interface states can be as low as that for SiO_2/Si [8, 9, 11]. This approach offers the potential for fabricating Ge nMOSFETs [8, 12, 13].

The process for fabricating Ge MOSFETs is becoming sufficiently mature and reproducible to warrant research into their reliability and some encouraging results have been reported [7, 14, 15]. Good TDDB data were obtained [14], but electron trapping is high [16], similar to that in the early stage of developing high-k/SiON stack for Si [17-20]. For Si-based CMOS technologies, the negative bias temperature instability (NBTI) is the most severe reliability issue, since it results in a lifetime of pMOSFETs shorter than that of nMOSFETs [21, 22]. With Si-capped Ge MOSFETs, it has been reported that NBTI can be lower than its Si counterpart [2, 14, 15, 23]. For the Ge pMOSFETs without a Si-cap layer, however, there is little information available on the NBTI.

The **central objective** of this work is to provide the information on the NBTI of Ge pMOSFETs with a $Ge/GeO_2/Al_2O_3$ structure. The results will be compared with both Si/SiON, Si/SiON/high-k stacks, and Si-capped Ge MOSFETs and similarities and differences will be highlighted. The dependence of NBTI on both stress field and temperature is investigated. Attention will be paid to the defects responsible for NBTI and the relative contribution from generated interface states will be estimated. It is found that the positive charges (PCs) in the oxides on Ge and Si behave differently and, when measured by either the conventional slow DC or pulse I-V technique, the conventional lifetime prediction method developed for Si based on the constant power exponent is not applicable to Ge pMOSFETs used in this work. A defect energy switching model is proposed to explain the differences.

II. DEVICES AND EXPERIMENTS

The gate dielectric stack used for the majority of tests in this work is shown in Fig. 1(a). The Ge layer is 700 nm and grown directly on Cz–Si wafers. To minimize interface states, a 1.2 nm GeO_2 was prepared by exposing clean Ge surface to an atomic oxygen flux at a low temperature of 150 ^oC for 20 min. A 4 nm Al_2O_3 was then produced by molecular beam deposition in the same chamber [24], resulting in a SiO_2 equivalent oxide thickness of 2.35 nm for the stack. Although Al_2O_3 only has a modest dielectric constant, it can suppress the evaporation of GeO and, in turn, the deterioration of GeO_2/Ge interface [25]. The device was annealed post-metallization in forming gas at 350 ^oC for 20 min. The channel length used in this work is typically 1 μm and the width is 50 μm. The pMOSFETs have a 10 nm PVD TiN metal gate. For the purpose of comparison, other structures used include

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Ge/Si-cap/SiO_2/HfO_2, Si/SiON/High-k, and Si/SiON and their details will be given in figure captions or legends.

The test follows the standard 'stress-and-sense' procedure [26, 27] and a typical Vg waveform is given in Fig. 1(b). To monitor the threshold voltage shift, i.e. ΔVth, the stress was periodically interrupted and the source current, i.e. Is, instead of Id, versus Vg was recorded under a drain bias of Vd = -100 mV by using a Vg ramp to minimize the impact of junction leakage. ΔVth was extracted from the Vg shift at a constant Is = 100 × W / L nA [28].

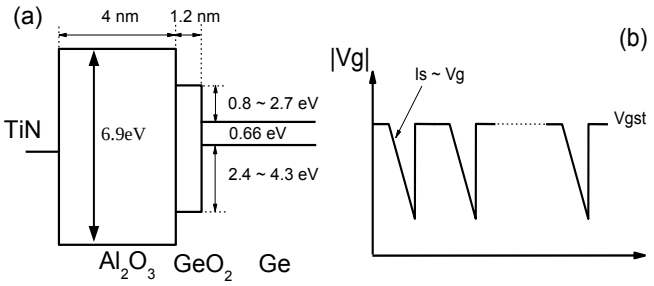

Fig. 1 (a) Schematic energy band diagram and structure of the used sample. (b) The gate bias waveform used in tests. Vgst is the stress bias.

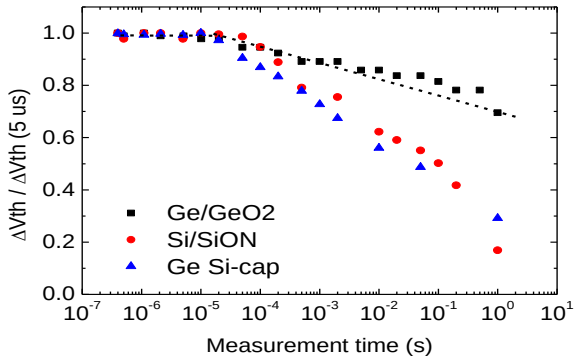

Fig. 2 Dependence of ΔVth on the measurement time for different samples. The stress field over the interfacial layer is 6.5 MV/cm for Ge/GeO_2 and 10 MV/cm for both Si/SiON and Si-capped Ge sample. The stress time is 1 ks and temperature is 20 °C. During the measurement period, Vg was kept negative and did not reach zero, as shown in Fig. 1(b).

The temperature used is in the range of 20 ~ 125 °C and the stress and measurement were performed at the same temperature, unless otherwise specified. The electric field over the interfacial GeO_2 layer was calculated from Eox=(Vg-Vth)×3.9/(6×EOT), where EOT is the SiO_2 equivalent thickness and the GeO_2 has a dielectric constant of 6 [29].

The measurement time, tm, can be defined as the time for sweeping Vg from the stress level Vgst to the measurement Vg for Is = 100 × W / L nA (see the ramp in Fig. 1(b)). Reliable measurements were obtained only for tm>0.4 μs and the recovery for shorter time could not be assessed. Fig. 2 shows that the recovery is negligible when tm increases from ~0.4 μs to ~10 μs and tm=5 μs is used here to minimize recovery. When tm=1 sec, recovery lowers ΔVth by 70~80% for Si/SiON and the Si-capped Ge sample, but only ~30% for Ge/GeO_2/Al_2O_3, so that ΔVth is relatively stable for the latter.

In this work, both tm=5 μs [27, 30] and tm=1 sec [31-33] were used. Although tm=5 μs minimizes recovery, agreement has not been reached on the NBTI kinetics even for Si/SiON[34-36]. Under the conventional slow DC measurement of tm=1 sec, however, it is widely accepted that ΔVth follows a power law and the Vg-accelerated lifetime prediction method is established [37] and some industrial researchers preferred tm=1 s (e.g. [38]). It is of importance to find out whether this method is applicable for Ge/GeO_2/Al_2O_3.

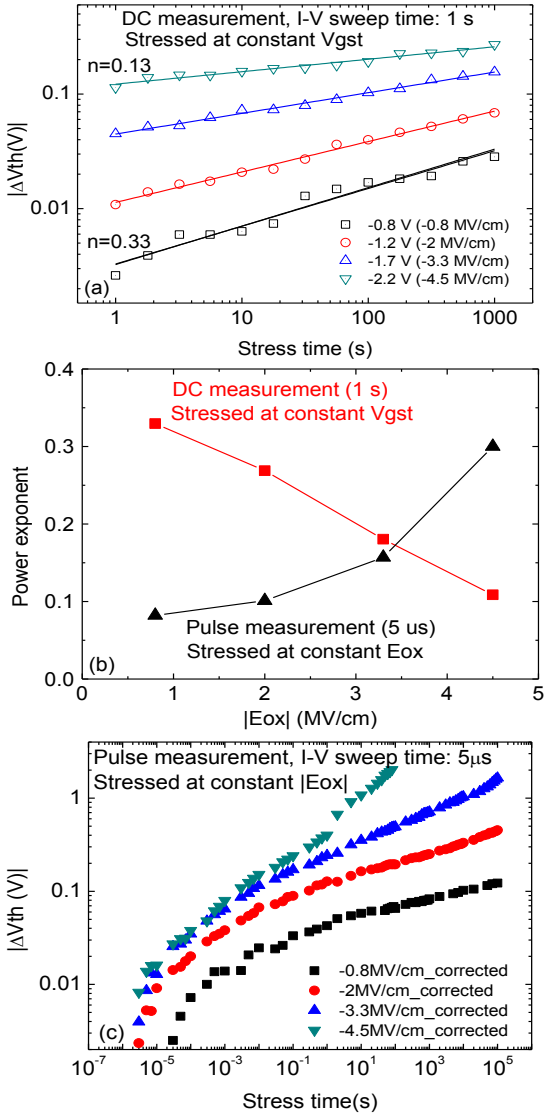

Fig. 3 (a) NBTI degradation kinetics under different stress biases at 20 °C measured by slow DC I-V of tm= 1 s. The solid lines were fitted with a power law. The stress Vg does not change with time and Eox in the legend is the field strength over GeO_2 at the start of stress. (b) The time exponent at different Vgst for DC and Eox for pulse measurement extracted within the time range of 1 s to 1000 s. (c) NBTI kinetics under constant stress Eox at 20 °C measured by pulse I-V of tm=5μs. The stress |Vg| was increased with time to maintain a constant Eox, here.

III. RESULTS AND DISCUSSIONS

A. NBTI under different stress fields

The Vg-accelerated lifetime prediction method for Si/SiON requires the time exponent of ΔVth to be independent of the stress Vg [27, 37]. When using this method, the stress bias, i.e. Vgst, typically does not change with time and tm is ~seconds. We applied these test conditions first to the Ge/GeO_2/Al_2O_3 and

Fig. 3(a) shows that ΔVth was substantial even under an operational bias level of -1.2 V (Eox=-2 MV/cm) and it is Vg-accelerated. The defect density in the current $Ge/GeO_2/Al_2O_3$ is clearly too high to meet the lifetime required for commercial application. It is of interest, however, to study their properties and dynamics, since the past experiences from high-k/SiON stack on Si show that the nature of the defects does not change when their density reduces substantially through process optimization [39, 40].

Although Fig. 3(a) appears similar to the conventional Si/SiON where ΔVth follows a power law against stress time [27], log|ΔVth| versus log(time), however, is not a parallel shift for different Vgst and the time exponent, n, reduces from 0.33 at Vgst=-0.8 V to 0.13 at Vgst=-2.2 V in Fig. 3(b), despite that the |Eox|≤4.5 MV/cm used here is well within the range typically used for Si MOSFETs when observing a constant time exponent [27, 41].

A possible explanation for the lower n at higher Vgst is that, when the stress was carried out under constant bias Vgst, the formation of positive charges lowers the |Eox| near the Ge/dielectric interface. At higher Vgst, there are more PCs, leading a larger reduction in |Eox| near Ge, lowering |ΔVth| and in turn n. This PCs-induced |Eox| reduction can be corrected by increasing $Vgst_i$ for a stress step i from the Vgst at the start of stress by ΔVth_{i-1}, so that the effective stress bias, (Vgst-Vth), and Eox is kept constant. To suppress the recovery during measurement and the consequent underestimation of ΔVth, tm=5 μs was used and Fig. 3(c) gives the result under constant stress Eox. The degradation does not follow a power law with a single exponent over the whole range of test time in Fig. 3(c), although data between 1 and 1000 sec can be fitted with a power law. The time exponent extracted between 1 and 1000 sec is given in Fig. 3(b), which increases for higher |Eox|. As a result, suppressing recovery during measurements and stressing under constant Eox do not lead to a constant time exponent and the conventional lifetime prediction method cannot be used for the $Ge/GeO_2/Al_2O_3$ used here.

B. Effects of stress temperature and anneal

Fig. 4(a) shows the ΔVth under |Vgst-Vth0|=0.75 V for different stress temperatures with tm=1 s. As expected, the NBTI is thermally activated. Under a higher |Vgst-Vth0|=2.35 V, however, Fig. 4(b) shows that ΔVth tends to become insensitive to temperature as it rises. This leads to a reduction of the activation energy, Ea, for higher Vgst, as shown in Figs. 4(c) and 4(d). Ea was extracted from the Arrhenius plot at 1000 sec in Fig. 4(c). It is an apparent activation energy with the measurement made at the stress temperature [42]. The insensitivity of ΔVth to temperature over 75 °C at |Vgst-Vth0|=2.35 V in Fig. 4(b) is not caused by running out of defects, since the longer stress clearly shows that the degradation can be higher.

The temperature-insensitivity of ΔVth at a stress time of 1000 sec has not been observed for Si/SiO_2 [43] and Si/SiON/High-k [44] and is worth of further exploring. One possibility is that the recovery during the 1 s measurement delay is also a thermally activated process, compensating the degradation. Figs. 5(a)-(d) give the results measured with tm=5 μs that minimized the recovery. The ΔVth appears insensitive to temperature initially (e.g. < 1 ms) and the reason is not known at present. For longer stress time, however, it is clearly thermally enhanced and the apparent Ea taken at 1000 sec is insensitive to Eox in Fig. 5(d).

To study the anneal of PCs**,** a device was exposed to 150 °C after stressing at 20 °C. Fig. 6(a) shows that nearly all PCs can be neutralized in 1800 sec. In comparison, the neutralization is less than half for Si/SiON under similar anneal conditions [45]. The following speculation is made to explain this difference.

It has been reported that the positive charges in SiO_2 can have energy levels above the bottom edge of the Si conduction band, i.e. Ec, making them difficult to reach by free electrons from Si substrate [17, 31-33]. The Ec offset between SiO_2 and Si is around 3.2 eV, so that these traps can be located well above the Si Ec. The Ec offset between GeO_2 and Ge, however, has been reported to be as low as 0.8 eV [46], so that the positive charge in GeO_2 should be closer to Ge Ec, making them relatively easier to neutralize at elevated temperature.

It is worth pointing out that the PCs in SiO_2 can only be fully neutralized when the anneal temperature reached 400 °C [45, 47]. After the anneal, the ΔVth in the subsequent stress becomes smaller than that before anneal, because of defect losses and slowdown in SiON [45, 47]. To test if this is also the case for $Ge/GeO_2/Al_2O_3$, the device was re-stressed after anneal and Fig. 6(b) clearly shows that ΔVth has not been reduced for the re-stress, so that the defect losses and slowdown were not observed here.

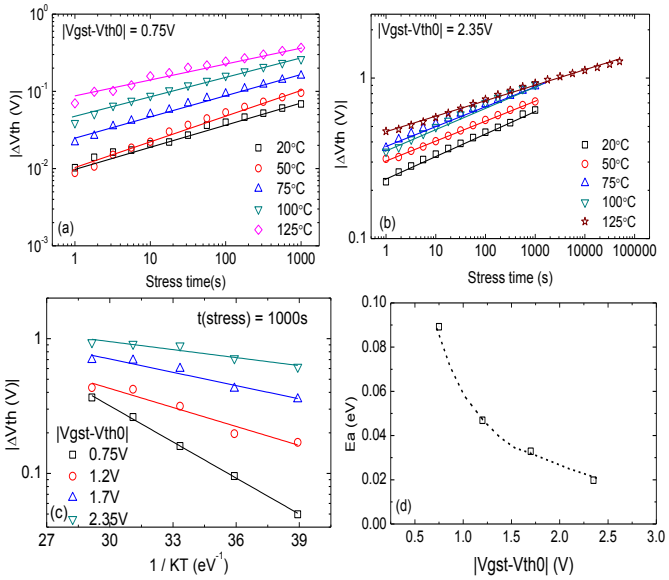

Fig. 4 NBTI kinetics under different stress temperatures, tm=1 s, and |Vgst-Vth0|=0.75V (a) and 2.35V (b). (c) is the Arrhenius plot at 1000 sec. (d) gives the extracted apparent activation energy from (c) at different |Vgst-Vth0|.

C. Contribution of generated interface states

The positive charges responsible for NBTI can originate from both the bulk of gate oxide and the oxide/substrate interface [22, 39, 43, 48]. When NBTI was reported for thick SiO_2 (e.g. 95 nm) in early years, the stress Eox was relatively

low and it was observed that PCs from the oxide and the interface were equally important [43]. For thin (< 3 nm) oxides, however, the stress Eox used is typically higher (e.g. 10 MV/cm) and hole injection occurs [22, 27]. The charging of hole traps leads to a larger contribution of PCs from oxides to ΔVth than that from generated interface states [22, 30, 49]. Nitridation introduces additional hole traps, further enhancing the contribution of PC from oxides to ΔVth [50, 51]. We now assess the relative importance of PCs from interface states for Ge pMOSFETs of a GeO_2/Al_2O_3 stack.

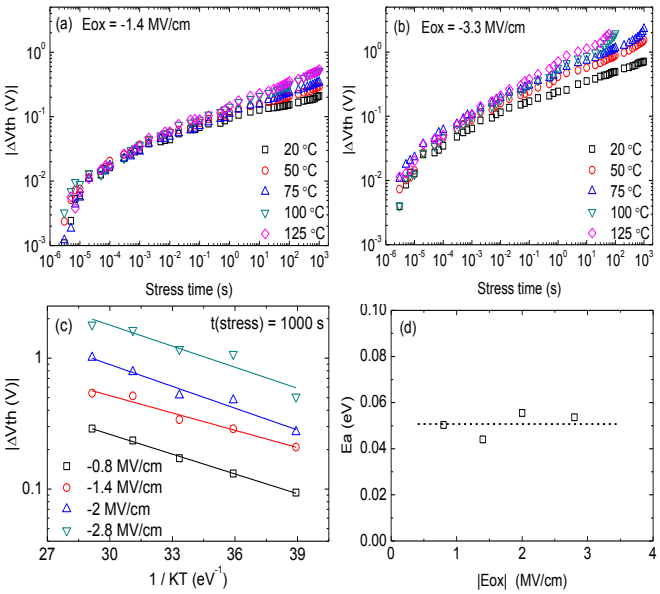

Fig. 5 NBTI kinetics under different stress temperatures with tm= 5 µs. The Eox during stress was kept at a constant of -1.4 MV/cm (a) and -3.3 MV/cm (b). (c) is the Arrhenius plot at 1000 sec. (d) gives the extracted apparent activation energy from (c) at different Eox.

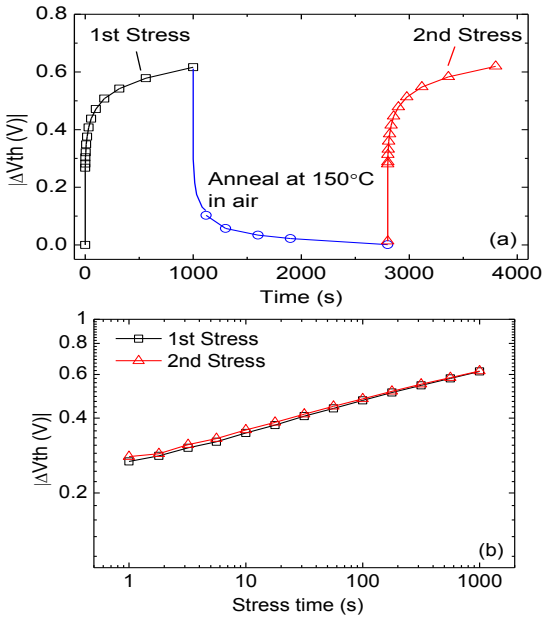

Fig. 6 (a) The 1st stress was under Vg= -2.8 V, 20 °C for 1000 s. The device was then annealed for 20 min at 150 °C in air with all terminals floating. The 2nd stress was under the same conditions as the 1st one. (b) compares the ΔVth for these two stresses by resetting the stress time to zero at the start of the 2nd stress. tm= 1s.

Fig. 7(a) presents a typical result of charge pumping measurements before and after a stress. The generation of interface states clearly can be seen from the raised peak after stress, resulting in an increase of interface state density of ΔDit = 1.88 × 10^{11} $cm^{-2}eV^{-1}$. As a first order estimation of the contribution from ΔDit to ΔVth, we assume a uniform energy distribution of interface states. It has been reported that the charge neutrality level is in the lower half of the bandgap for Ge [52], but, for simplicity, we assume that all states between the mid-band and Ev are donor-like and contribute to positive charges. This gives rise to a positive charge of ΔNit = 0.33 × ΔDit = 6.20 × 10^{10} cm^{-2} and a corresponding threshold voltage shift of ΔVit = ΔNit × q / Cox [53]. Fig. 7(b) compares the ΔVit with the measured ΔVth, showing that ΔVit is one order of magnitude smaller.

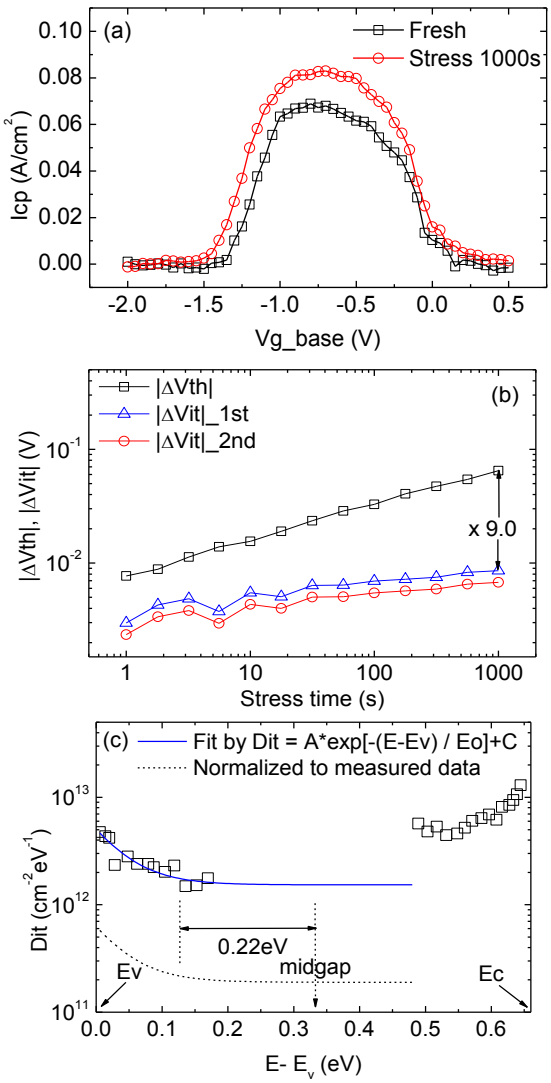

Fig. 7 (a) The charge pumping current, Icp, before and after a stress under Vgst = -1.2 at 20 °C. (b) A comparison of the 1st and 2nd order estimated contribution of enerated interface states to the threshold voltage shift with the measured ΔVth. (c) The energy distribution reported in ref. [29]. The dashed line is obtained by normalizing the solid line to the measured 1.88 × 10^{11} $cm^{-2}eV^{-1}$ in the range of 0.22 eV from midgap. The charge pumping amplitude is 1V, frequency is 1 MHz and the rise and fall time is 20 ns.

The ΔDit measured by CP is the average value over an energy range of ± 0.22 eV centered at midgap in our case [54]. It has been reported that the interface state density rises substantially towards the band edge, so that an assumption of uniform energy distribution can underestimate the contribution of ΔDit. As a second order approximation, we use the energy profile reported in earlier work [29] for Dit. As shown in Fig. 7(c), the solid curve was fitted with the test data by using an expression, Dit = A × exp[-(E-Ev) / Eo] + C, where A, Eo and C are constants. This function was then normalized to the measured ΔDit over the energy range from midgap to 0.22 eV below it, resulting in the dotted line in Fig. 7(c). The positive charges were estimated by integrating the dotted line between midgap and Ev, resulting in $\Delta Nit = 7.89 \times 10^{10}$ cm^{-2}. The corresponding ΔVit is also shown in Fig. 7(b) and its contribution remains insignificant. The stress in Fig. 7 was at 20 °C. At 125 °C, the measured ΔVit (not shown) can be twice as high as that at 20 °C, but it is still only about $1/8^{th}$ of the total ΔVth. We conclude that the NBTI of $Ge/GeO_2/Al_2O_3$ is dominated by positive charges in the dielectric.

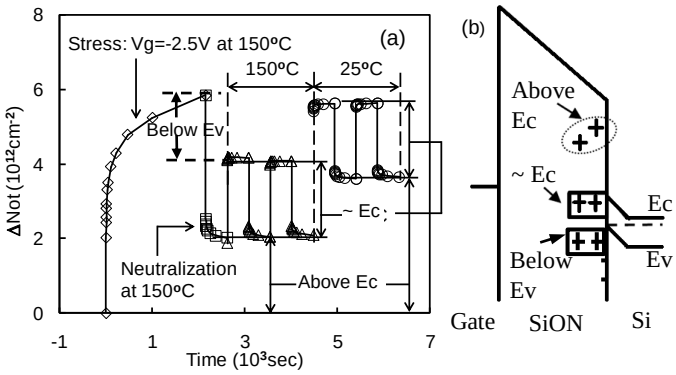

Fig. 8 (a) Different types of PCs in $Si/SiON/HfO_2$. After stress and neutralization, Eox = ± 5MV/cm were applied with alternating polarity to show the traps ~Ec and above Ec at 150 °C and then 25 °C [47]. Vg>0 V reduces ΔNot and Vg<0 V increases PCs. (b) illustrates the energy level differences for the three types of PCs. ΔNot was measured from the Id-Vg shift at midgap, where interface states are neutral for Si MOSFETs.

D.Positive charges in dielectric: energy switching model

It has been shown in Section III-A and B that NBTI in the Ge sample behaves differently from that in Si samples. In this section, the cause for these differences will be investigated at the defect level. For Si pMOSFETs, the positive charges (PC) in gate oxides have a complex behavior and have been explained differently by different groups [27, 30, 36, 54-57]. Figs. 8(a)&(b) summarize their typical behavior and one way of characterizing them is to separate them into three groups according to their energy ranges: hole traps below the Si Ev, around Si Ec, and above Si Ec [17, 22, 31-33, 44]. After building up PCs during stress at high |Eox|, substantial neutralization occurs under Vg>0 at a relatively low Eox = 5 MV/cm. By alternating the polarity of Eox = ± 5 MV/cm, traps around Si Ec can be repeatedly charged and neutralized, and those well above Ec remain charged and are not neutralized. Most traps below Si Ev cannot be re-charged under Eox = - 5 MV/cm. In the following, we will show that PCs in GeO_2/Al_2O_3 on Ge are different.

Fig. 9 shows a typical result for GeO_2/Al_2O_3 on Ge. Although the first impression is that the PCs behave similarly to those in Si samples, a close inspection, however, reveals several important differences:

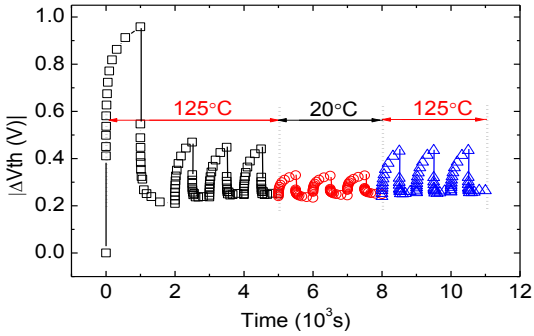

Fig. 9 Positive charges in $Ge/GeO_2/Al_2O_3$ device. The stress was at Vgst = -2.6 V and 125 °C, After a neutralization step at +4.2 MV/cm at 125 °C, Eox = ± 3.3 MV/cm were applied with alternating gate polarity in a temperature sequence of 125 °C, 20 °C, and 125 °C. The time for switching temperature is 40mins with gate floating and this time was not included in the time axis.

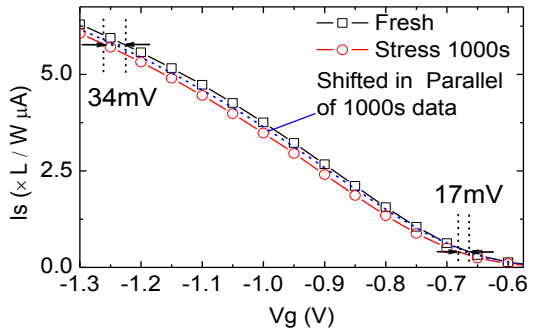

Fig. 10 Is - Vg before and after stress under Eox = -6.5 MV/cm for 1000 s on a Si/SiON/HfO/AlO device. The dotted line is a parallel shift of the line for 1000 sec data until it reached the fresh Is - Vg at low |Vg|. It shows the stressed Is - Vg is not in parallel with the fresh Is - Vg.

- The charge and neutralization of traps around Ec by alternating Vg polarity for Si samples in Fig. 8(a) is insensitive to measurement temperature, i.e. T, since it has an energy level accessible even at room temperature and the charge and neutralization are through carrier tunneling here that is a process insensitive to T. In contrast, Fig. 9 shows that the charge/neutralization cycling in Ge sample reduces for lower T.
- The density of PCs in traps above Ec in Si samples in Fig. 8(a) clearly increase at lower T. After being neutralized at a higher T, the defect energy level remains above Ec. As soon as T is reduced, electrons leave the defects, tunnel into the Si conduction band, recharge the defects, and result in the higher PCs. For the Ge sample, however, Fig. 9 shows that the remaining PCs hardly increase when the temperature lowers from 125 °C to 20 °C.
- When Vg sweeps from the stress level in the positive direction to a sensing Vg, some traps in Si samples fall below the Fermi level and are neutralized [22, 27, 30]. Fig. 11 shows that |ΔVth| nearly halved when Vg moves from -1.2 V to -0.6V. In contrast, the change of ΔVth with Vg is

much smaller for Ge samples (Fig. 11), indicating detrapping from traps below Ev for Ge is less important than that in Si.

The above differences indicate that the PCs in Ge samples are different from those in Si samples, so that a different model is needed. We propose an 'energy switching model' to explain these differences. The first-principle calculations show that energy levels of a defect in dielectric can strongly depend on its charge states [58, 59]. The 'energy switching' here means that the energy level of a defect switches from one value to another, when its charge-state changes. As illustrated in Fig. 12(a), neutral hole traps have a spread of energy levels below Ev of Ge. Application of higher |Eox| allows charging the traps further below Ev, leading to the field activation of NBTI in Fig. 3(a). Application of higher temperature also charges the hole traps further below Ev, resulting in the higher ΔVth at higher temperatures in Figs. 4 and 5.

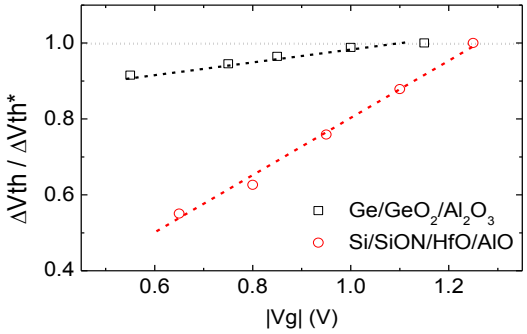

Fig. 11 Dependence of ΔVth on the sensing Vg. ΔVth* is the ΔVth measured at the highest sensing |Vg| for a sample. Devices were stressed under an initial Eox = -6.5 MV/cm for 1000 s at 20 °C.

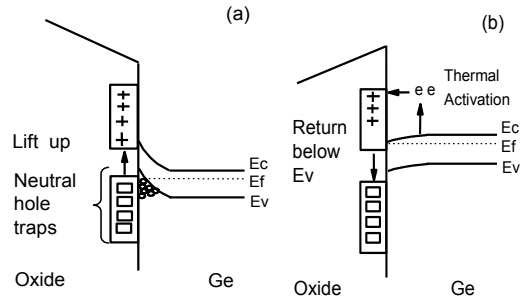

Fig. 12 The energy-switching model for positive charges in $Ge/GeO_2/Al_2O_3$. (a) shows charging under Vg < 0, (b) shows neutralization under Vg > 0. '□' represents neutral hole traps and '+' represents charged hole traps.

After being charged, instead of staying at the same energy level, the defects are lifted to energy levels well above Ge Ev. This allows most hole traps holding their PCs when Vg is swept from stress toward threshold levels, giving rise to the smaller reduction in Fig. 11, when compared with that in Si/SiON

If the energy levels of the lifted PCs were near Ec, their neutralization should be insensitive to temperature, similar to those in Si samples in Fig. 8. Fig. 9 shows that this is not the case for Ge samples, however. On the other hand, if the lifted PCs are above Ec, their neutralization should be thermally enhanced, as illustrated by Fig. 12(b), similar to the PC above Si Ec in Fig. 8(b) [17, 31, 44]. This is confirmed below.

Fig. 13 shows that an increase of T clearly lowers ΔVth for both Si (Fig. 13(a)) and Ge (Fig. 13(b)) samples. The thermal activation of neutralization supports the proposition that there are PCs above the Ge Ec. However, when T reduces subsequently, ΔVth rises back for Si, but remains the same for Ge samples. This supports the view that, unlike the case of Si samples, the energy level of defects drops back below Ev after neutralization at high T to prevent recharge at the subsequent low T for Ge sample without re-stress, as illustrated in Fig. 12(b). Because the energy level was switched below Ev after neutralization at 125 °C, lowering temperature to 20 °C did not recharge them, unlike the Si sample in Fig. 13(b).

For Ge sample at a time t*, a signature of the energy-switch after neutralization is that the number of un-neutralized PC is determined by the highest temperature a sample was exposed prior to t*, rather than the temperature at t*. In contrast, for Si sample, the lack of energy level switching means that the number of un-neutralized PC at t* is determined by the temperature at t*. In another word, one may say that $Ge/GeO_2/Al_2O_3$ can remember its temperature history, but Si/SiON cannot. The underlying physical mechanism for the energy switching is not known. One speculation is the field-assisted multi-phonon emission during hole trapping [55] and further evidences are needed to support it.

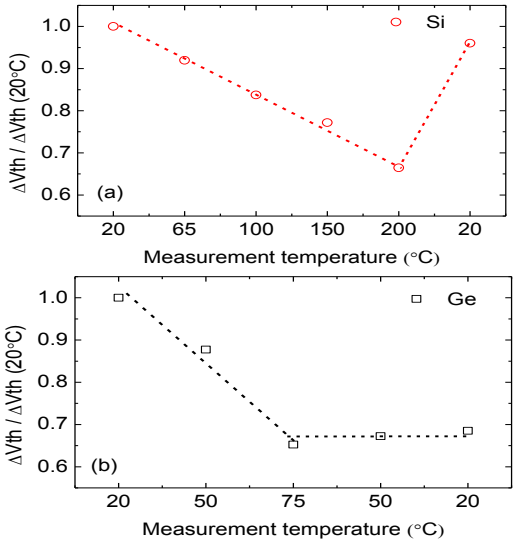

Fig. 13 Impact of measurement temperature on ΔVth for (a) Si/SiON and (b) $Ge/GeO_2/Al_2O_3$. The lines are a guide for the eye. tm= 1s.

IV. Conclusions

This work characterizes the NBTI for $Ge/GeO_2/Al_2O_3$ and compares it with Si samples. Similar to Si samples, NBTI is activated both electrically and thermally for $Ge/GeO_2/Al_2O_3$. There are a number of important differences with Si samples and the new findings include: (i) The time exponent is not constant for different stress biases/fields when measured with either slow DC or pulse technique, which makes the conventional Vg acceleration lifetime prediction technique of Si samples inapplicable to the $Ge/GeO_2/Al_2O_3$; (ii) ΔVth is

substantially less sensitive to measurement time; (iii) The neutralization can be nearly 100% under a temperature as low as 150 ^{o}C, in contrast with the 400 ^{o}C needed by Si sample. (iv) Defect losses were not observed for $Ge/GeO_2/Al_2O_3$.

On defects, the positive charges in GeO_2/Al_2O_3 on Ge dominate the NBTI. They do not follow the same model as that for PCs in SiON/Si and an energy-switching model has been proposed: the energy levels have a spread for neutral hole traps below Ev, lift up after charging, and return below Ev following neutralization. Finally, we point out that these conclusions are drawn based on the samples used in this work and their generic applicability awaits further tests.

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