A framework for defects in PBTI and hot carrier ageing

Jian Fu Zhang*, Meng Duan, Zhigang Ji, and Weidong Zhang

Department of Electronics and Electrical Engineering, Liverpool John Moores University, Liverpool L3 3AF, UK * Email: j.f.zhang@ljmu.ac.uk

Abstract

Both positive bias temperature instability (PBTI) and hot carrier ageing (HCA) are major challenges to the reliability of modern CMOS technologies. This work reviews the recent progresses in understanding the defects. An as-grown-generation (AG) framework is proposed, based on the energy profile, charging kinetics and generation. Three types of electron traps are identified: As-grown cyclic electron traps (ACET), generated cyclic electron traps (GCET), and generated anti-neutralization electron traps (ANET). PBTI only has ACET and ANET, while HCA also causes GCET and create new interface states. This lays the foundation for modelling PBTI and HCA.

1. Introduction

For modern CMOS technologies, positive bias temperature instability (PBTI) is a major reliability issue and hot carrier ageing (HCA) is limiting the maximum use bias and device lifetime [1,2]. Despite of the extensive research in both of them, the similarity and differences in their defects are not clear and a framework is in need. This work reviews the latest progress in our understanding and proposes an As-grown-Generation (AG) framework for the defect [2-6].

The framework is established based on an investigation of the energy profile, charging and discharging properties, and generation. It will be shown that there are three different types of electron traps: As-grown cyclic electron traps (ACET), generated cyclic electron traps (GCET), and anti-neutralization electron traps (ANET). PBTI only has ACET and ANET and hot carriers are needed to generate GCET. In terms of energy location, ACET is shallowest and ANET is the deepest. The charging kinetics of ACET and GCET are dramatically different: ACET follows power law, while GCET saturates in seconds.

2. Devices and experiments

nMOSFETs were fabricated by a bulk 28 nm CMOS process. The devices have a metal gate and high-k stack with an equivalent oxide thickness of 1.2 nm. The channel length and width are 36 nm and 900 nm, respectively.

All tests were carried out at 125 °C. PBTI and HCA was performed under Vd=0 and Vd=Vg, respectively.

The ageing was periodically monitored by interrupting the stress and the threshold voltage shift, ΔV th, was measured from the Vg shift under a fixed drain current of 100 nA×W/L, which was taken from the pulsed Id-Vg under Vd=0.1 V [7-11].

3. Electron traps under PBTI

The test procedure is given in Fig. 1a. A relatively low gate voltage +1.5 V was applied first and the stage_1 in Fig. 1a shows that the charged electron traps can be fully discharged by the following Vg= -1.8 V. Charge-discharge can be cycled by alternating Vg=+1.5 and -1.8 V, so that they are referred to as 'As-grown Cyclic Electron Traps (ACET) [2-6].



Fig. 1. (a) Test procedure of ACETs and ANET. Stage_1 alternates Vg between 1.5 and -1.8 V to monitor the as-grown cyclic electron traps (ACET). At stage_2, a heavy stress was applied with Vg=2V, followed by discharge at Vg=-1.8 V. Stage_3 repeat Stage_1. (b) compares CET at Stage_1 and _3. by removing ANET. [3]

In stage_2, a higher Vg=2V was applied and the increased stress induces a higher PBTI. When Vg= -1.8V was applied, some traps were not neutralized and they are called as Anti-neutralization electron traps (ANET). In the following stage_3, the same biases as those in the stage_1 were re-applied. The cyclic electron traps (CET) in the stage_1 and _3 are compared in Fig. 1b and they agree well. This susports that PBTI does not generate additional CET and the CET observed in the stage_1 is as-grown.



Fig. 2. The test procedure is similar to that in Fig. 6(a). In stage_1, the distribution was measured after charging PCET at Vg=1.8 V for 1 ks. Then a heavy PBTI stress under 2 V was applied. After full discharge, in stage_3, CET was recharged at 1.8 V and the distribution was measured again. (a) compares the trap density before and after the heavy PBTI stress. (b) was obtained by removing ANETs and (c) shows the CET energy profile is not changed by the heavy PBTI stress. [3].

The discharge-based energy profile technique [12,13] is used in Fig. 2. The ACET has a single peak

near 1.4 eV and it does not change after heavy PBTI stress.

To study ANET further, Fig. 3 shows that the subthreshold swing (SS) does not degrade after PBTI, so that there is no interface state generation [14]. The ANET must be the created electron traps.



Fig. 3. A comparison of subthreshold swing (SS) degradation under PBTI and HCA. SS does not degrade for PBTI, suggesting no interface states created. Clear SS degradation is observed after HCA stress. Inset shows the SS extraction method. [3].



Fig. 4. (a) The HCA is used in the stage_2. The bias conditions in the stage_1 and _3 are the same as those in Fig.1a. (b) compares the ACET at stage_1 and CET at stage_3 by removing ANET+Nit. A clear increase of CET is observed, due to the generated electron traps (GCET). [3].

4. Electron traps under Hot Carrier Ageing

In Fig. 4a, the PBTI in the stage_2 of Fig. 1 was replaced by HCA under Vg=Vd=+2V. The bias conditions in the stage_1 and _3 are the same as those in Fig. 1a. The ANET of HCA is much higher than that of PBTI. Fig. 3 shows that HCA degrades SS and there are interface state generation [14]. In addition, CET becomes higher after HCA and the differences in the two sets of CETs in Fig. 4b are the generated CET (GCET).

The energy distribution is given in Fig. 5. The GCET has a clear peak at 1.6 eV, 0.2 eV deeper than the ACET.



Fig. 5. (a) compares the trap density before and after heavy HCA stress. (b) was obtained by removing ANETs. (c) shows energy profile of both GCET and PCET. GCET peaks at 1.6 eV, 0.2 eV deeper than that for the original PCET. [3].

5. Charge kinetics of ACET and GCET

The charge kinetics of ACET follows power law in Fig. 6a. After HCA, the total CET in Fig. 6b may appear also follow power law, but this is an art-fact. After subtracting ACET, Fig.6c shows that charging GCET completes in seconds. This clear difference between ACET and GCET strongly support that they are different types of defects, although both of them are cyclic.

The dependence on charging Vg is given in Fig. 7.

GCET saturates near 1.5 V, while no saturation can be observed for ACET.



Fig. 6. Charging kinetics of PCET (a) and total CET (b) under different Vg. PCET under Vg=0.9V is negligible and not shown in (a), however after HCA stress CET under Vg=0.9V is significant in (b). (c) The difference between (a) and (b), i.e., the GCET. [3].



Fig. 7. Dependency of ACET and GCET on charging Vg. At an operation voltage of 0.9 V, GCET is one order magnitude more than ACET. [3].

6. A framework for defects

An as-grown-Generation (AG) framework is summarized for electron traps in Fig. 8. It consists of one type of as-grown cyclic electron traps (ACET) and two types of generated electron traps: generated cyclic electron traps (GCET) and anti-neutralization electron traps (ANET).

Both PBTI and HCA charge ACET. As Fig. 7 shows that ACET charging is negligible under Vg=+0.9 V, they must located well above Si Ec when neutral. After charging, however, their energy level in Fig. 8 is below Si Ec. This means that ACETs are energy alternating defect: charging lowers its level and neutralization raises it. The power law charging kinetics could originate from the structure relaxation during trapping.

GCET are generated by HCA, but not by PBTI. Once generated, GCET can be charged by either PBTI or HCA. Like ACET, their energy level also lowers following charging with a peak 0.2 eV deeper than ACET. Unlike ACET, their charging saturates in seconds, possible because the low barrier between the two wells in Fig. 8c.

ANET are generated by both PBTI and HCA. They have deeper energy levels (>1.8 eV) than ACET and GCET. In addition, HCA also generates interface states, while PBTI does not.



Fig. 8. (a) A schematic illustration of new AG model. ACET peaks at 1.4 eV below Ec of HK, GCET peaks at 1.6 eV, and ANET locates deeper than 1.8 eV. Two wells model of ACET (b) and GCET (c). Charging rate of ACETs can be limited by the energy barrier between two wells. However this barrier is insignificant for GCET.

7. Summary

Based on the energy profile, charging kinetics, and generation, an as-grown-generation (AG) framework is proposed for defects in PBTI and HCA. Both PBTI and HCA charge the as-grown cyclic electron traps (ACET) and generate anti-neutralization electron traps (ANET). In addition, HCA creates new cyclic electron traps (GCET) and new interface states. ACET is located at 1.4 eV and GCET at 1.6 eV. ACET charging follows a power law, while GCET charging saturates in seconds. These differences must be taken into account when modelling PBTI and HCA.

Acknowledgments

The authors would like to thank A. Asenov of Glasgow University, D. Vigar of Qualcomm Technologies International Ltd, V. Chandra, and R.

Aitken of Arm Holding, and B. Kaczer and G. Groeseneken of IMEC for useful discussions. The test samples used in this work were supplied by D. Vigar. This work is supported by the EPSRC of UK under the grant no. EP/L010607/1.

References

[1] A. Bravaix, Y. M. Randriamihaja, V. Huard, D. Angot, X. Federspiel, W. Arfaoui, P. Mora, F. Cacho, M. Saliva, C. Besset, S. Renard, D. Roy, E. Vincent, IRPS, pp 2D.6.1-2D.6.9, 2013.

[2] M. Duan, J. F. Zhang, A. Manut, Z. Ji, W. Zhang, A. Asenov, L. Gerrer, D. Reid, H. Razaidi, D. Vigar, V. Chandra, R. Aitken, B. Kaczer, and G. Groeseneken, IEDM Tech. Dig., pp. 547-550, 2015.

[3] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, D. Vigar, A. Asenov, V. Chandra, R. Aitken, B. Kaczer, IEEE Trans. Elec. Dev., vol. 63, pp. 3642-3648, 2016.

[4]. J. F. Zhang, Z. Ji, W. Zhang, Microelectronics Rel., vol. 80, pp. 109-123, 2018.

[5] Z. Ji, S. F. W. M. Hatta, J. F. Zhang, J. G. Ma, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, IEDM Tech. Dig., pp. 413-416, 2013.

[6] Z. Ji, J. F. Zhang, L. Lin, M. Duan, W. Zhang, X. Zhang, R. Gao, B. Kaczer, J. Franco, T. Schram, N. Horiguchi, S. De Gendt, and G. Groeseneken, IEEE VLSI Tech. Symp., pp.36-37, 2015.

[7] Z. G. Ji, J. F. Zhang, M. H. Chang, B. Kaczer, and G. Groeseneken, IEEE Tran. Elec. Dev., vol. 56, pp. 1086-1093, 2009.

[8] Z. Ji, L. Lin, J. F. Zhang, B. Kaczer, and G. Groeseneken, IEEE Trans. Elec. Dev., vol. 57, pp. 228-237, 2010.

[9] L. Lin, Z. Ji, J. F. Zhang, W. D. Zhang, B. Kaczer, S. De Gendt, and G. Groeseneken, IEEE Trans. Electron Dev., vol. 58, pp. 1490-1498, 2011.

[10] J. F. Zhang, M. H. Chang, Z. Ji, L. Lin, I. Ferain, G. Groeseneken, L. Pantisano, S. De Gendt, and M. M. Heyns, IEEE Electron Device Letters, vol. 29, pp.1360-1363, 2008.

[11] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, B. Kaczer, T. Schram, R. Ritzenthaler, A. Thean, G. Groeseneken, and A. Asenov, IEEE VLSI Tech. Symp., pp.74-75, 2014.

[12] S. F. Wan Muhamad Hatta, Z. Ji, J. F. Zhang, M. Duan, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, IEEE Trans. Electron Dev., vol. 60, pp. 1745-1753, 2013.

[13] J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. Chalker, IEEE Elec. Dev. Lett., vol. 35, pp.162-164, 2014.

[14] M. H. Chang, and J. F. Zhang, J. Appl. Phys., vol. 101, art.no. 024516, 2007.