A Source and Drain Transient Currents Technique for Trap Characterisation in AlGaN/GaN HEMTs

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***Abstract*—The source/drain and gate induced charge trapping within an AlGaN/GaN high electron mobility transistor is studied, under normal device operation, by excluding self-heating effects, for the first time. Through direct measurement of current transients of both source and drain terminals, a characterisation technique has been developed to: (i) analyse the transient current degradations from µs to seconds, and (ii) evaluate the drain and gate induced charge trapping mechanisms. Two degradation mechanisms of current are observed: bulk trapping at a short time (<1ms); and surface trapping and redistribution (>1ms). The bulk charge trapping is found to occur during both ON and OFF states of the device when V_{DS}>0V; where its trapping time constant is independent of bias conditions. In addition, the time constant of the slower current degradation is found to be mainly dependent on surface trapping and redistribution, not by the second heat transient**.

Keywords—AlGaN/GaN HEMTs; Transient Currents; Traps Characterisation; Self-Heating Effects.

I. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are predicted to significantly improve efficiency and to dominate applications, e.g. high-power, high-frequency, low-noise, ultra-wide-band communication, ultra-scaled high-temperature, wireless sensors, etc., because of III-Nitrides' wide-bandgaps, high electron saturation velocities and good thermal conductivities [1], [2]. In recent years, these devices have been steadily improving and new record performances have been reported each year [3], [4]. However, their reliability issues persist due to a lack of understanding of physics and mechanisms of charge trapping, self-heating and polarisation [5]–[8].

Several studies investigating the current degradation in AlGaN/GaN HEMTs have resulted in differing conclusions [8]–[10]. It is widely agreed upon that transient current degradation involves self-heating and charge trapping, [11]–[14]. Some studies of transient drain current suggest that two mechanisms of current degradation of different time constant are caused by both bulk and surface trapping [8], [9]. Other investigations suggest that the two current degradation trends are proportional to self-heating effects that occur at two different times [10]. With the significant impact of the current degradation time constant and magnitude on device reliability and RF performance, it is vital to address its mechanisms and origins.

The aim of this work is to gain insights into the degradation mechanisms of AlGaN/GaN HEMTs, focusing on both source and drain transient current measurements and analyses. We confirm that two current degradation mechanisms occur. At a short time scale (<1ms), the RF performance is restricted by both bulk trapping and self-heating effects. At a longer time scale (>1ms), the dynamic ON resistance degradation is limited mainly by surface trapping accumulation and redistribution. The used device structure and experiment methodology are summarised in Section II, while Section III outlines the results on source and drain current transient measurements, I_S and I_D, for both degradations. Conclusions are drawn in Section IV.

II. Devices And Experimental Procedure

A. Device Structure and Fabrication

The investigated epi-structure of the AlGaN/GaN HEMT was grown by molecular beam epitaxy (MBE) on HP-Si [111] substrate of a resistivity of 2000Ω.cm, as shown in Fig. 1a. MBE was performed using NH_3 for the Nitrogen precursor. The HEMT structure consists, from the substrate to the top, of low-temperature AlN/GaN/AlN (250/250/40nm) nucleation layers, a 1.1µm GaN back-barrier and 1nm AlN exclusion layer to reduce alloy scattering and to improve the carrier confinement of the 2-D Electron Gas (2DEG). A 25nm undoped $Al_{0.28}Ga_{0.72}N$ barrier and, finally, a 1nm undoped GaN cap layer. Room temperature Hall measurements yields a sheet resistance of R=340Ω/sq, an electron sheet density of $1.25\times10^{13}cm^{-2}$, electron mobility of $1480cmV^{-1}s^{-1}$, and

dislocation density of ~5×10^{9}cm^{-2}. The gate metallisation scheme is Ni/Pt/Ti/Mo/Au (5/25/25/30/250nm), where Ti/Al/Ni/Au (10/200/40/100nm) multilayers were used for the source and drain terminals. The contact resistance and specific resistivity are 0.39Ω.mm and 3.8×10^{-6}Ω.cm^2, respectively. The fabrication process flow is similar to that in [15] with additional Si_3N_4 passivation. The I_{DS}-V_{DS} at V_{DS}=20V and I_D-V_G at V_{GS}=0V characteristics of the used AlGaN/GaN HEMT are plotted in Fig. 1a.

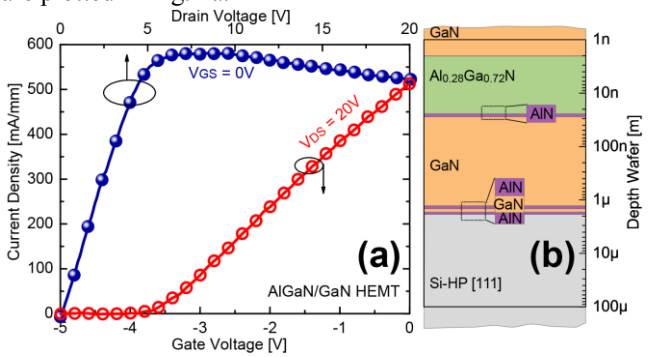

Fig. 1: (a) I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics at V_{GS}=0V and V_{DS}=20V, respectively, of the used AlGaN/GaN HEMT. (b) Schematic cross-section of the epi-structures grown on Si-HP [111] substrate. The source-to-drain distance and device width are 5µm and 100µm, respectively.

B. *Experimental Methodology*

In order to investigate the charge trapping involved in the AlGaN/GaN HEMT structure, we propose two experiments. The pulse waveforms, given in Fig. 2a, were used to characterise the bulk trapping mechanism. Here, V_{DS}=0V and V_{GS}=0V were pulsed to V_{DS1} and V_{GS1}, respectively, for a measurement time of $t_{meas,1}$=1s. The pulse waveforms, given in Fig. 2b, were used to investigate surface trapping behaviour. Quiescent biasing conditions, V_{DSQ} and V_{GSQ}, were set whereby pre-charging of surface trapping occurred. Measurements were then taken at V_{DS2}=10V and V_{GS2}=0V for a time $t_{meas,2}$=1s. An illustration is provided in Fig. 2c showing both bulk and surface trapping mechanisms.

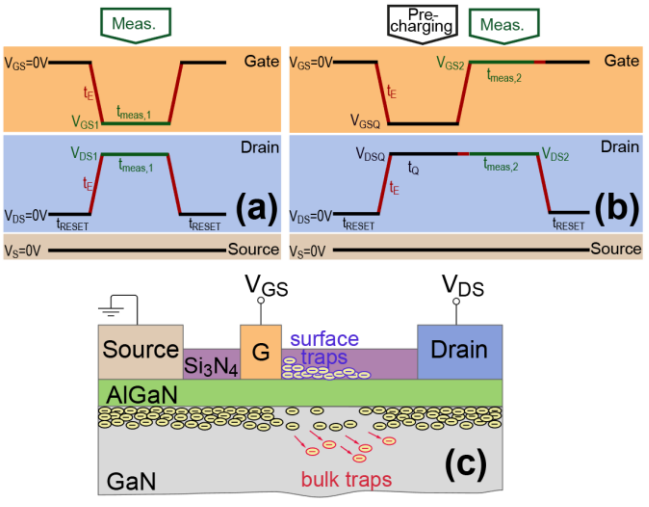

Fig. 2: Pulse waveforms used for I_S and I_D transient measurements for: (a) without traps pre-charging and (b) with traps pre-charging, where t_{RESET}=10s and t_E=200ns. (c) The schematic diagram of bulk and surface trapping mechanisms are illustrated for a semi-ON-state at V_{DS}>0V.

III. Results And Discussion

A. *Bulk Trapping Mechanism*

For the first time, experimental measurements of both source and drain transient currents were analysed to understand charge trapping kinetics under normal device operation. To attain this, the experiment illustrated in Fig. 2a was used. Fig. 3 shows the current transients, I_S and I_D, monitored at V_{DS1}=20V various gate biases, V_{GS1}=0V to -3V. Measurements were also taken for V_{DS1}=10V and V_{DS1}=15V (not shown). Under high V_{DS1}, a large peak in electric field at the drain-side of the gate is induced. As a result, electron trapping in the drain access region of the device increases channel resistance [16]. Considering this, the transient behaviour of I_S and I_D can be broadly split into two phases:

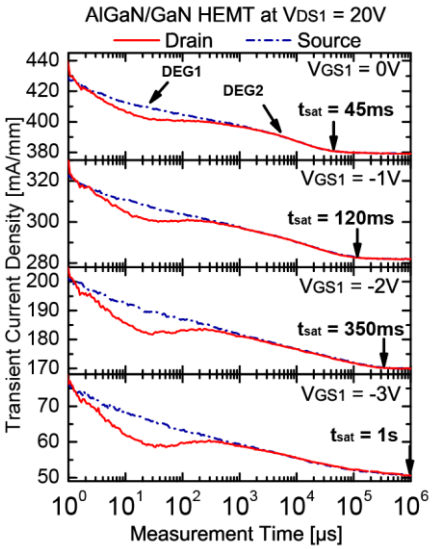

Fig. 3: Transient behavior of the drain, I_D, and source, I_S, currents, versus measurement time on log scale using the pulse waveforms given in Fig. 2a with V_{DS1}=20V, at V_{GS1}=0V to -3V. Two degradations of current are observed at different time constants, DEG1 and DEG2.

- *A fast initial charge trapping phase (≤1ms) – DEG1*: Bulk traps are identified as the fast charge trapping mechanism that contributes to the first degradation mechanism (DEG1) [6]. Electrons that exit the source terminal and become trapped within the bulk are not collected by the drain terminal, resulting in a difference between I_S and I_D. Whilst this occurs, the device heats up over time due to the applied electric field, causing both I_S and I_D to degrade proportionally. I_S and I_D difference is also seen when conditions of Fig. 2a are applied to an AlGaN/GaN Transmission Line Model (TLM) gateless device (not shown). This indicates that the difference between I_S and I_D is not caused by gate terminal.
- *A slow current degradation phase (>1ms) – DEG2*: During this phase, negligible difference between I_S and I_D is observed and, therefore, negligible bulk trapping occurs. The slow degradation of current (DEG2) is due to a surface trapping and/or a second phase of self-heating [10],[17]. For this reason, the impact of surface trap redistribution compared to the second self-heating mechanism is investigated in section B.

To analyse the effect of the bias conditions on the initial charge trapping phase (DEG1), the difference between I_S and I_D (I_S-I_D) under V_{DS1}=10V, 15V and 20V at different gate biases, V_{GS1}=0V to -3V were measured (Fig. 4a). We find that a significant increase in bulk trapped charge density, indicated by the increase of $(I_S\text{-}I_D)_{max}$ from 3.8mA/mm to 7.0mA/mm, is observed when V_{DS1} is increased from 10V to 20V (Fig. 4b). However, there is no change in trapped charge density upon increasing the magnitude of V_{GS1}. Also, bulk trapping time constant is shown to be independent of V_{DS} and V_{GS}.

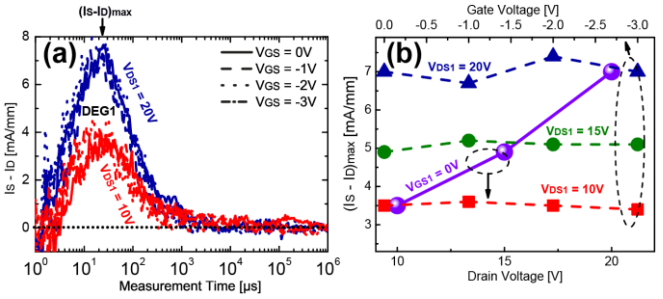

Fig. 4: (a) I_S and I_D difference (I_S-I_D) versus the measurement time at V_{DS1}=20V and 10V for different gate voltages (V_{GS1}=0V to -3V); indicating the bulk trapping process (DEG1). (b) The impact of drain voltage, V_{DS1}, and gate voltage, V_{GS1} on $(I_S\text{-}I_D)_{max}$ given at t≈30µs; unlike V_{DS1}, V_{GS1} shows a negligible impact on bulk trapping characteristics.

With respect to the slow current degradation phase, DEG2, there is no change in bulk trapping as I_S is very close to I_D. Yet, a second current degradation is still observed, which could be a result of surface trapping and/or self-heating. In the following section, the mechanism of DEG2 is investigated.

B. Surface Trapping Mechanism

To investigate the effect of the bias conditions on DEG2, the saturation time, t_{sat}, of Fig. 3 is extracted and plotted in Fig. 5a. It is clear that t_{sat} can be influenced by both V_{GS1} and V_{DS1}. On one hand, the increase of $|V_{GS1}|$ induces greater surface trapping density, leading to a larger time for redistribution. On the other, the required time to redistribute the trapped electrons at the surface and extend the 'virtual gate' towards the drain side reduces when increasing V_{DS1}. Larger V_{DS1}, higher electric field, provides more energy to surface traps to distribute quicker [18]. The redistribution of surface traps alter the potential distribution laterally in the device, which affects the channel resistance.

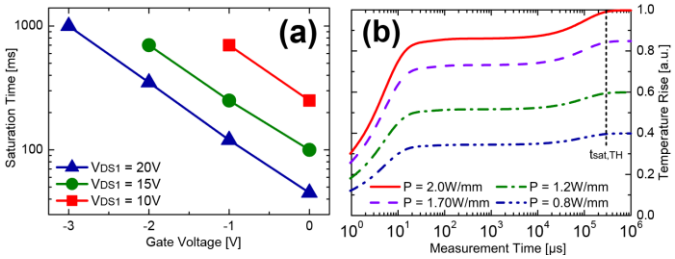

Fig. 5: (a) Saturation time of DEG2, t_{sat}, at V_{DS1}=20V, 15V, and 10V and V_{GS1}=0V to -3V; showing the dependence of t_{sat} with both V_{DS1} and V_{GS1}. (b) transient heating at various power densities (P) using the RC thermal model [10], [19]. It is noted that $t_{sat,TH}$ is temperature independent.

Taking advantage of the RC thermal model, it appears that the second phase of self-heating has no influence on t_{sat}, as illustrated in Fig. 5b [10], [19]. We observe that $t_{sat,TH}$, corresponding to the time saturation of the second transient heating is completely independent of temperature. Therefore, t_{sat} is mainly affected by surface trapping. We conclude that the surface trapping is the primary cause that affects the time constant of the current degradation DEG2, when the device is operating in the semi-ON state.

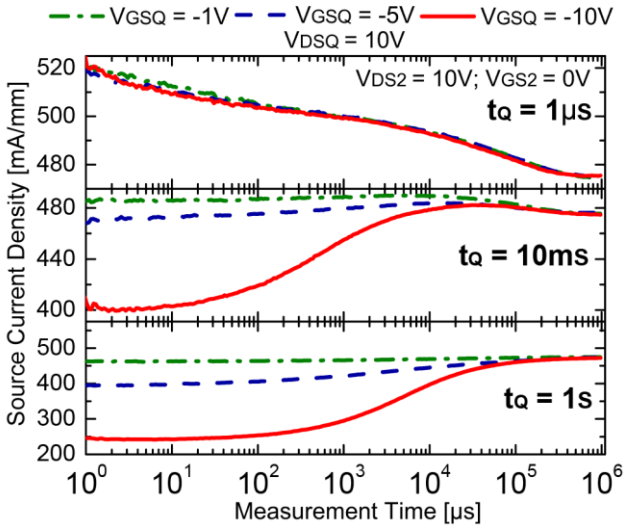

Fig. 6: Recovery of current, measured at V_{DS2}=10V and V_{GS2}=0V (Fig. 2b), after various pre-charging conditions are applied: V_{GSQ}=-1V, -5V, and -10V, at V_{DSQ}=10V, for a period t_Q=1µs, 10ms, and 1s. The recovery in the current transients at t_Q≥10ms shows the dominance of surface trapping on device degradation over self-heating.

To investigate the impact of bias conditions on the current degradation DEG2 during the OFF-state, we applied the pulse waveforms shown in Fig. 2b. A trap pre-charging condition is applied before measuring the transient currents. During the pre-charging time window, surface trapping and redistribution are induced by V_{GSQ} and V_{DSQ}, respectively. During this pre-charging condition, no self-heating occurs, since the device is in the OFF-state. When the pre-charging time, t_Q, is greater than 1ms, the bulk trapping saturates during the pre-charging period at the same amount as in Fig. 4a. As consequence, a negligible further bulk trapping is observed during the measurement phase (not shown).

Fig. 6 shows the source current transient, I_S, monitored at V_{DS2}=10V and V_{GS2}=0V. Here, different bias conditions for the trap pre-charging (V_{GSQ}=-5V and -10V at V_{DSQ}=10V) are applied for t_Q=1µs, 10ms, and 1s, and $t_{meas,2}$=1s, respectively. A pre-charging at a semi-ON state, V_{GSQ}=-1V, is also used for a comparison purpose. As the measurement condition, V_{DS2} and V_{GS2}, is applied, both surface trapping and redistribution begin to recover. This occurs due to the detrapping of the pre-charged electrons when the gate voltage magnitude is decreased from $|V_{GSQ}|$ to $|V_{GS2}|$. As a result, 'virtual gate' length decreases and channel resistance is reduced; thereby recovering current.

For pre-charging time, t_Q≥10ms, the device heats up during the measurement window, yet the current recovers. This shows the dominance of the surface trapping recovery over the self-heating degradation. This dominance diminishes with decreased V_{GSQ} as there is less current recovery observed. As the pre-charging time, t_Q, is reduced, there is less surface trapping and redistribution during the pre-condition. For

example, at t_Q=1µs, much less recovery is observed during measurement. Regardless, surface trapping is still shown to be dominant for pre-conditions where $t_Q \geq 10$ms and $|V_{GSQ}|>5$V and it can cancel out self-heating induced current reduction at $|V_{GSQ}|=0$V.

IV. Conclusion

In this paper, a new source and drain transient currents, I_S and I_D, technique for charge trapping characterisation in AlGaN/GaN HEMTs, under normal device operation, has been developed. Using this technique, charge trapping behaviours, with the exclusion of self-heating, have been analysed. Two types of charge trapping mechanisms have been identified: (i) bulk trapping occurring on a time scale of <1ms, followed by (ii) surface trapping and redistribution beyond 1ms. The bulk trapping and surface trapping corresponds to fast and slow current degradations, respectively.

Through monitoring the difference between I_S and I_D, bulk trapping time constant is shown to be independent of V_{DS} and V_{GS}. Although, V_{DS} is found to affect the bulk trap density. Large V_{DS} is found to be a cause of bulk charge trapping during both ON and OFF states of the device. The time constant of the slower current degradation is found to be mainly dependent on surface trapping and redistribution. This time constant increases with higher $|V_{GS}|$ and lower V_{DS}.

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