PREDICTIVE AS-GROWN-GENERATION MODEL FOR NBTI OF ADVANCED CMOS DEVICES AND CIRCUITS

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ABSTRACT

Increasing pressure on the quest towards low power applications with stringent reliability demands requires narrowing the gap between NBTI models and real circuit operation for design optimization. In this work, we reviewed the recent-proposed As-grown-Generation (AG) model. By separating different types of defects through experiment, we demonstrated that it can make reliable prediction beyond the measurement window. Compared with other existing models, the proposed model delivered its original mission: Reliably predicting long term aging at low Vg based on a model extracted from Vg-accelerated short tests. Its simple formula makes it readily implementable for circuit level simulation.

INTRODUCTION

Negative bias temperature instability (NBTI) is a well-known reliability issue which can has impact on CMOS integrated circuits [1]. Although firstly reported in 1966 [2], it is only during the last ten years that NBTI became the most serious reliability issue due to the increase of the gate electric field and chip operating temperature with scaling and the routinely introduction of nitrogen adding to the gate dielectric [3]. Modeling the negative bias temperature instability (NBTI) is essential for optimizing circuit design. Several models have been proposed [4-6]. They are usually physical-based and are validated by fitting with the test data. The drawbacks are two-fold: a) There is still no agreement on physical mechanism yet; b) By increasing the number of parameters, the apparent success of the model could be just the consequence of good fitting of existing data and thus have little use in predicting the unknown circuit operating condition. There is a pressing need for a NBTI model to reliably predicting long term NBTI at low use-bias, based on a model extracted from Vg-accelerated short tests.

In this work, a defect-based As-grown-Generation (A-G) model is proposed to model the NBTI-induced degradation. Through separating different types of defects directly from the measurement, the framework shows good predictive capability for long term degradation under any given voltages. The work is arranged as follows: The details about the devices is described in Section II. Then in Section III, we will show how different types of defects can be experimentally separated. Based on the extracted kinetics, the A-G model will be proposed and validated in section IV. Finally, it comes to the conclusion of the paper.

DEVICES AND EXPERIMENT

pFinFETs fabricated using a Hf-based high-k oxide and a metal gate are used to demonstrate the proposed model. The EOT is sub-1-nm with TiN metal gate [7]. Fast measurement with the Id-Vg measured within 3μs is used [8]. The threshold voltage degradation is monitored by sensing at a constant Id of 500nA*W/L around threshold voltage. Unless specified, the temperature is 125 °C.

Although NBTI is considered as electric-field driven phenomenon [3], the tests were usually performed under the constant Vg. The underlying assumption is that the total degradation, ΔVth, is much smaller than the applied voltage. **Fig.1** compared the NBTI degradation under the constant-Vg and constant-E condition, wherein, constant-E is approximately achieved by consistently increasing stress bias, Vgst, by the amount of ΔVth, which is measured in the last step. Clear difference can be observed between the two, indicating that the electric filed has been affected by the ΔVth. In this work, unless specified, the constant-E test will be applied.

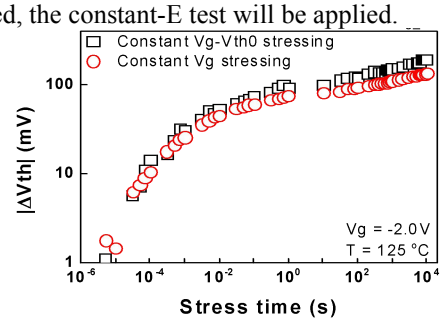

Fig. 1 The comparison between the constant Vg and constant Eox paradigms for NBTI.

As-GROWN-GENERATION (A-G) FRAMEWROK

The pre-existing defects and the generated defects have been considered as two main types of defects contributing in NBTI. The former are those already exist in the dielectric, while the latter require much higher voltage to create in the first instance. To model NBTI correctly, it is important to characterize and understand the kinetics of each defect, as will be elaborated below.

i. Generated defects (GD)

Clear experiments, such as SILC [9] and charge pumping [10] strongly support the existence of GD. It is usually extracted by arbitrarily taking the last point at the end of the recovery trace [11], making it sensitive to the measurement conditions such as. discharging time, tdisch, and the discharge voltage, Vgdisch. To understand this phenomenon, the energy distribution of defects [12] are

extracted from the device in fresh and after 1ks stress, as shown in **Fig.2a**. Subtracting the fresh from the stressed one gives the distribution of GD component, as shown in **Fig.2b**. Clearly, GDs are located both within the Si bandgap and beyond Si conduction band. In favor of the energy level, those GD within the bandgap can be charged and discharged repeatedly, so that they are referred to as cyclic positive charges (CPC). On the other hand, the defects above Si Ec are more difficult to neutralize and they are called as Anti-Neutralization positive charges (ANPC), as shown in **Fig.2c**.

Fig.3a&d shows ANPC reduces against either Tdisch or Vgdisch. However, the same amount of the increase can be observed in CPC in **Fig. 3b&e**. This can be understood that the discharged ANPC can be refilled and thus be accounted into CPC. The total GD, i.e. GD=CPC+ANPC in **Fig.3c&f**, is independent of Tdisch and Vgdisch. Based on the understanding, the Stress-Discharging-Recharging (SDR) procedure can be used to capture the kinetics of the entirety of GD, as shown in **Fig.4** [13]: After stressing under Vgst for a certain time, the measurement starts by applying an opposite polarity of Vgdisch to accelerate the discharge of pre-existing traps. Then the low use-bias under real operation Vgch (|Vgch|< |Vgst|) was applied to refill all the traps that contribute under use condition. By subtracting the measured degradation with the same recharging step but on fresh device, GD can be obtained. **Fig. 5** shows the measured GD kinetics under different overdrive voltage, Vgov. GD follows power law relationship against time and can be well described with the classical power law using Eqn (1) for long term prediction. Wherein, g0, m and n are the pre-factor, voltage and time exponent respectively. The time exponent is 0.2.

$$GD = g_0 \cdot V_{gov}{}^{m} \cdot t^{n} \quad (1)$$

ii. Pre-existing defects

Pre-existing defects originate from the fabrication imperfectness. their charging and discharging kinetics will not be affected by the device's stress history. Therefore, they can be characterized using heavily stressed devices.

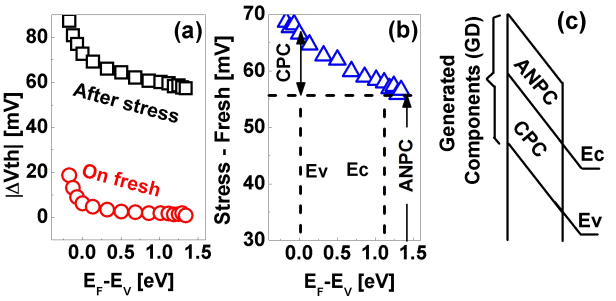

Fig. 2 (a) Comparison of the energy profiles before and after stress. **(b)** The profile for GD extracted substracting two curves in (a). **(c)** Illustration of the energy range for the cyclic positive charges (CPC) and the anti-neutralization positive charges (ANPC).

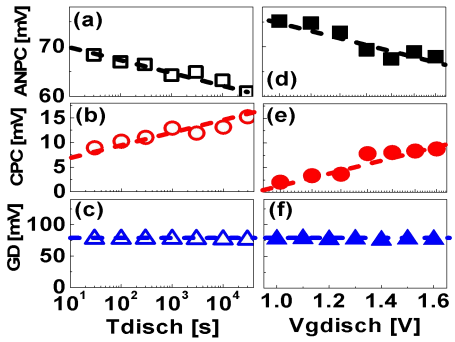

Fig. 3 Dependence on discharge conditions for **(a&d)** ANPC, **(b&e)** CPC and **(c&f)** GD=ANPC+CPC. The discharging voltage is +1.6V. Wherein, ANPC equals to Vth(end of discharge) – Vth(Fresh), CPC equals to Vth(end of recharge) – Vth(end of discharge) and GD is the sum of ANPC and CPC.

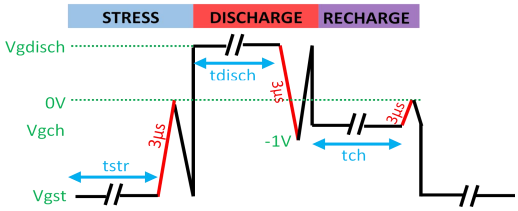

Fig. 4 The test follows a stress-discharge-recharge sequence. At the end of each step, ΔVth was monitored from a corresponding Id~Vg, taking from the 3μs pulse edge.

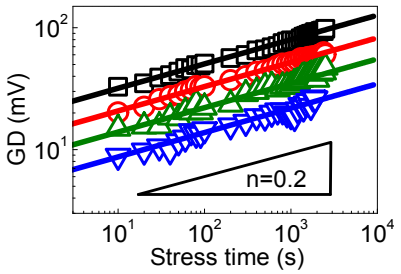

Fig.5 Generation kinetics of GD. The degradation follows power law with Vgov and time.

To understand these pre-existing traps, the energy profile is extracted after the device charging up under the bias, Vgch [14]. As shown in **Fig.6**, when Vgch is low, the profiles after filling at different Vgch overlap well. However, when Vgch increases further, they deviate from each other. This can be considered that two different types of hole traps in the gate dielectric, as illustrated in **Fig. 7a&b**: one type can capture a hole without changing its energy level. While another type, after capturing one hole, its energy level shift upwards from the ground state to the charged state, resulting in the increased ΔVth in **Fig.6** at a given Vgdisch-ΔVth, after filling at higher Vgch. One simple method can be applied to separate these two types of traps by exploiting the parallel region of the distributions extracted for two consecutive Vgch levels, as illustrated in **Fig. 8a**: starting with the distribution trace at the lowest Vgch in which only AT traps are involved, the

discharging trace under the next charging level, Vgch+ΔVgch, is shifted down to align these two curves within the tail region from the charging level. By following this procedure up to the highest Vgch, the distribution of saturated AT traps can be extracted from the experimental data and fitted empirically with Eqn(2), as shown in **Fig. 8b**. EAD traps can then be extracted by subtracting AT from the total, as shown in **Figs. 9**.

$$Saturated\_AT = p_1 \cdot \exp(p_2 \cdot V_{gov}) \quad (2)$$

The charging kinetics of EAD under different Vgov are shown in **Fig. 10**. EAD follows power law relationship in time and voltage and can be modelled with Eqn (3). It is important to note that although both EAD and GD follow power law relationship, they have different time exponent and thus need to be modelled separately. **Fig. 10a** shows the charging kinetics for AT under different Vgov, they all quickly reach saturation. When they are normalized against its saturated value, as shown in **Fig. 10b**, they follow the same stretched exponent kinetics as described by Eqn (4).

$$EAD = g_2 \cdot V_{gov}^{m2} \cdot t^{n2} \quad (3)$$

$$AT = Saturated\_AT \cdot [1 - \exp(-\frac{t_{AT\_ch}}{\tau})^{\gamma}] \quad (4)$$

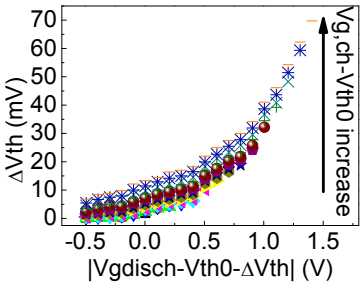

Fig. 6. Energy distribution of the Pre-existing trap after charging under different levels, *Vg*,ch for 1000 s at 125°C.

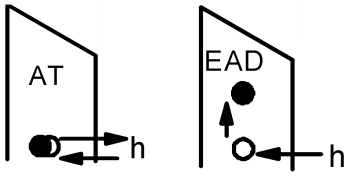

Fig. 7. Illustration of charging (a) AT and (b) EAD traps. AT do not change energy level while EAD will after charging.

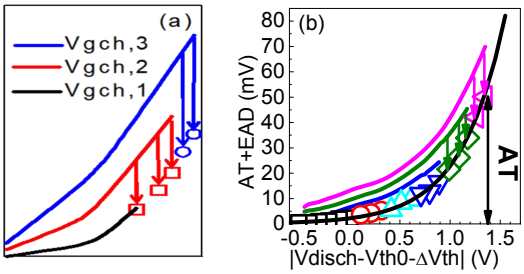

Fig. 8 (a) Illustration on extracting AT. **(b)** The method is applied to real data.

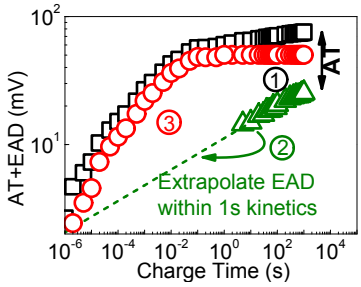

Fig. 9 EAD kinetics by subtracting total AT from total degradation. AT kinetics is obtained by subtracting EAD kinetics from the total.

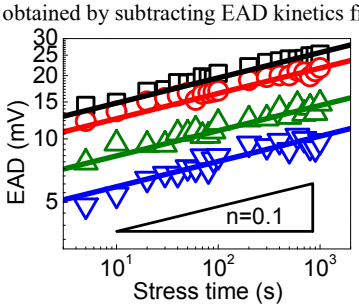

Fig.10 The charging kinetics of EAD: The degradation follows power law with Vgov and time.

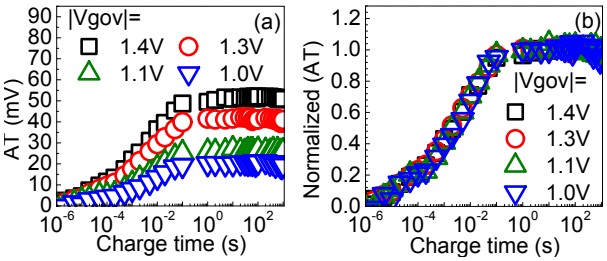

Fig. 11 (a) AT charging kinetics under different Vgov, it saturated in short time. **(b)** When they are normalized against its saturated value, it follows the same stretched exponent kinetics

It is widely accepted that charging and discharging of pre-existing traps dominates during AC operation. Therefore, the discharging kinetics is required, which can be measured at the end of charging under each Vgov. The discharging of the total pre-existing traps under different charging time or voltages are shown in **Fig.12a&b**. They can be scaled following universal recovery curve as shown in **Fig.12c** and described with Eqn (5).

$$f(t_{disch}) = (1 + B \cdot t_{disch}^{\beta})^{-1} \quad (5)$$

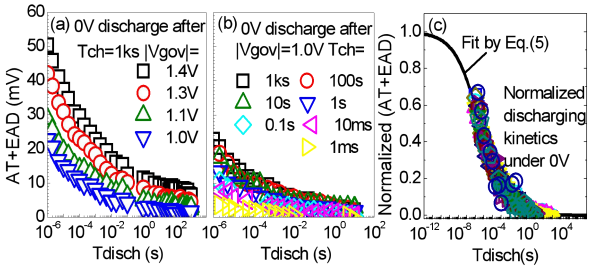

Fig. 12 Discharging kinetics of the pre-existing defect after different charge voltage **(a)** and charging time **(b)**. **(c)** They can be normalized with universal recovery trace as described in Eqn (5).

Model Prediction and Validation

Based on the knowledge of the defects involving in the NBTI degradation, an A-G simulator can be built on the Eqns (1) - (5) [15]. By solving these coupled equations, the NBTI degradation under both DC and AC operation mode can be predicted. To be practical useful, the model must has the predictive capability, i.e. the model parameters collected from short-term high stress conditions should be able to be used to predict the long-term degradation kinetics at devices' low operating condition. One demonstration is shown in **Fig. 13**. Four Vg-accelerated short DC stresses were firstly carried out to extract the A-G model, which then is used to predict the both DC and AC NBTI under use-Vg_ov. The good agreement between the prediction and the measurement can be observed, delivering the original mission of NBTI modelling.

It is intuitive to understand the contribution of each defect under operating condition. As shown in **Fig. 14**. For DC NBTI stress, it is obvious that there are more EADs compared with GD at the initial stage. However, due to the higher time exponent, GD increase much faster than EAD and plays more important role in the long term. For AC stress, since GD has negligible discharge at 0V while EAD discharges a lot, in a much earlier term GD has already surpassed EAD compared to DC case. AT is relative small compared with the other two components.

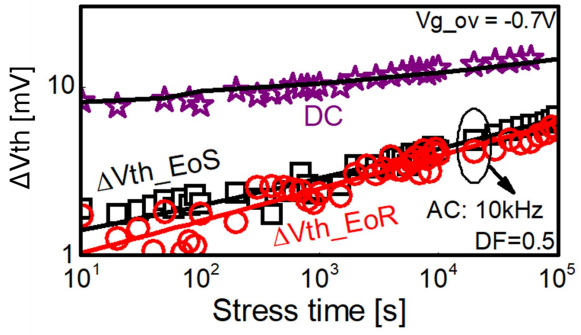

Fig. 13 Demonstration of the prediction capability for both DC and AC NBTI. The frequency and DF dependent after stressing for 1ks is compared between the prediction (lines) and test data (symbols).

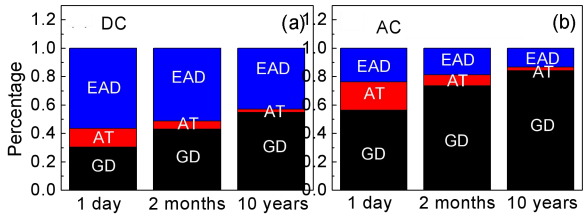

Fig. 14 Kinetics of different components against stress time under DC (a) and 1kHz (b) NBTI stress. The normalized contribution of different components under different stress time is given in (c) DC

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REFERENCES

[1] W. Wang, S. Yang, S. Bhardwaj, S. Vrudhula, F. Liu, and Y. Cao, "The Impact of NBTI Effect on Combinational Circuit: Modeling, Simulation, and Analysis," IEEE Trans. VLSI, p.173, 2010.

[2] B. E. Deal, M. Sklar, A. Grove, and E. Snow, "Characteristics of the Surface - State Charge (Qss) of Thermally Oxidized Silicon," J. Electrochem. Soc., p. 266, 1967.

[3] D. K. Schroder, "Negative bias temperature Instabilty: What do we understand?" Micro. Rel., p.841, 2007.

[4] S. Deora, V. D. Maheta and S. Mahapatra., "NBTI Lifetime Prediction in SiON p-MOSFETs by H/H2 Reaction Diffusion(RD) and Dispersive Hole Trapping Model," in *Proc. IRPS*, p. 1105, 2010.

[5] V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, and C. Ouvrard, "New characterization and modeling approach for NBTI degradation from transistor to product level," in *IEDM.*, p. 797, 2007,

[6] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P. J. Wagner, F. Schanovsky, J. Franco, M. Luque and M. Nelhiebel, "The paradigm shift in understanding the bias temperature instability: From reaction–diffusion to switching oxide traps," IEEE Trans. Electron Devices, pp. 3652, 2011.

[7] L, Ragnarsson, Z. Li, J. Tseng, T. Schram, E. Rohr, M. J. Cho, T. Kauerauf, T. Conard, Y. Okuno, B. Parvais, P. Absil, S. Biesemans and T. Y. Hoffmann, "Ultra low-EOT gate-first and gate-last high performance cmos achieved by gate-electrode optimization", IEDM p.1, 2009.

[8] Z. Ji, L. Lin, J. F. Zhang, B. Kaczer, and G. Groeseneken, "NBTI Lifetime Prediction and Kinetics at Operation Bias Based on Ultrafast Pulse Measurement," IEEE Trans. Electron. Dev. p. 228, 2010.

[9] J. Q. Yang, M. Masuduzzman, J. F. Kang and M. A. Alam, "SILC-Based Reassignment of Trapping and Trap Generation Regimes of Positive Bias Temperature Instability," in Proc. IRPS, p.196, 2011.

[10] L. Lin, Z. Ji, J. F. Zhang, W. Zhang, B. Kaczer, S. De Gendt and G. Groeseneken, "A Single Pulse Charge Pumping Technique for Fast Measurements of Interface States," IEEE Trans. Electron. Dev., p.1490, 2011.

[11] X. Wang, S.-H. Song, A. Paul, and C. H. Kim, "Fast characterization of PBTI and NBTI induced frequency shifts under a realistic recovery bias using a ring oscillator based circuit," in Proc. IRPS, p. 6B.2.1, 2014.

[12] Z. Ji, S. Hatta, J. F. Zhang, J. Ma, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, "Negative bias temperature instability lifetime prediction: Problems and solutions," in IEDM Tech. Dig., p. 15.6.1, 2013.

[13] R. Gao, A. B. Manut, Z. Ji, J. Ma, M. Duan, J. F. Zhang, J. Franco, S. W. M. Hatta, W. Zhang, B. Kaczer, D. Vigar, D. Linten, and G. Groeseneken, "Reliable time exponents for long term prediction of negative bias temperature instability by extrapolation," IEEE Trans. Electron. Dev., p.1490, 2017.

[14] P. P. Ren, R. Gao, Z. Ji, H. Arimura, J. F. Zhang, R. Wang, R. Huang, M. Duan, W. Zhang, J. Franco, S. Sioncke, D. Cott, J. Mitard, L. Witters, H. Mertens, B. Kaczer, A. Mocuta, N. Collaert, D. Linten, A. V.-Y. Thean, and G. Groeseneken, "Understanding charge traps for optimizing Si-passivated Ge nMOSFETs," VLSI-T, p.214 2015.

[15] R. Gao, Z. Ji, S. M. Hatta, J. F. Zhang, J. Franco, M. Duan, W. Zhang, B. Kaczer, S. De Gendt, D. Linten and G. Groeseneken, "Predictive, defect-centric As-grown-Generation (A-G) model for device/circuit co-design with nanoscale CMOS technology," VLSI-T p.355, 2016.