DEFECTS AND LIFETIME PREDICTION FOR GE PMOSFETS UNDER AC NBTI STRESSES

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ABSTRACT

Germanium has higher hole mobility and is a candidate for replacing silicon for pMOSFETs. This work reviews the recent progresses in understanding the negative bias temperature instability (NBTI) of Ge pMOSFETs and compares it with SiON/Si devices. Both Ge and SiON/Si devices have two groups of defects: as-grown hole traps (AHT) and generated defects (GDs). The generation process, however, is different: GDs are interface-controlled for SiON/Si and dielectric-controlled for Ge devices. This leads to substantially higher GDs under DC stress than under AC stress for Ge, although they are similar for SiON/Si devices. Moreover, GDs alter their energy levels with charge status and can be reset to original precursor states after neutralization for Ge, but these processes are insignificant for SiON/Si. The impact of these differences on lifetime prediction will be presented and the defects and physical mechanism will be explored.

INTRODUCTION

Hole mobility in Ge is ~4 times of that in Si, making Ge pMOSFETs faster than Si. The Negative Bias Temperature Instability (NBTI) of Ge devices varies substantially: the Si-capped Ge device can have longer lifetime than Si devices, while GeO_2/Ge has much shorter lifetime. This has attracted a lot of attentions [1-6] and a review will be given for the recent progresses in understanding the NBTI of Ge devices, based on the authors' works [2-6]. We will use SiON/Si devices as the benchmark and explore the similarity and differences between Ge and SiON/Si devices in terms of defects, generation mechanism, and lifetime prediction.

Table 1: Gate stack
a) 2.3nm or 2 nm plasma-N **SiON/Si**
b) 4nm Al_2O_3/1.2nm **GeO_2/Ge**
c) 2nmHfO_2/~0.4nmSiO_2/ **Si-cap/Ge**

DEVICES AND EXPERIMENTS

The gate stack used is given in Table 1. Tests follows the 'stress-and-sense' procedure [7,8]. After a preset stress time, a gate pulse with an edge time of 5 µs was applied and the threshold voltage shift, ΔVth, was measured at a constant source current of 100×W/L nA at Vd= -100 mV [7,8]. Unless otherwise specified, the tests were carried out at 125 °C.

NBTI DYNAMICS

To investigate the NBTI dynamics under both AC and DC stresses, the gate bias, Vg, waveform in Fig. 1 was used. Initially, AC stress was applied at a frequency of 10 kHz and a duty factor of 50%. This was followed by a DC stress, where Vg has the same value as the AC amplitude. Finally, the AC stress was reapplied.

1st AC stress -- DC stress -- 2nd AC stress

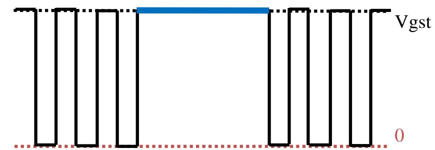

Fig. 1 The waveform of stress gate bias.

A typical result for SiON/Si devices is given in Fig. 2. When the AC stress was replaced by DC stress, Fig. 2a shows that NBTI become substantially higher [9]. As the AC stress was reapplied, however, the DC-enhanced degradation quickly recovers and Fig. 2b shows that NBTI kinetics returns to the same power law line, when plotted against "effective stress time", i.e. the AC stress time multiplied by its duty factor.

For Ge devices, Fig. 3a shows that the NBTI also increases substantially when switched to the DC stress and there is a recovery after AC stress was reapplied. Unlike the 'full recovery' in Fig. 2a, the recovery in Fig. 3a, however, is 'partial' and there is a substantial DC-induced 'additional generation' that did not recover, leading to an up-shift of the power-law in Fig. 3b [5]. To explain this difference, the generation process and defect properties will be explored.

GENERATION PROCESS AND DEFECTS

We have proposed that the NBTI in Si devices follows the As-grown-Generation (AG) model [10,11] that divides defects into two groups: As-grown hole traps (AHTs) and Generated defects (GD),

$$\Delta Vth = AHT + GD. \qquad (1)$$

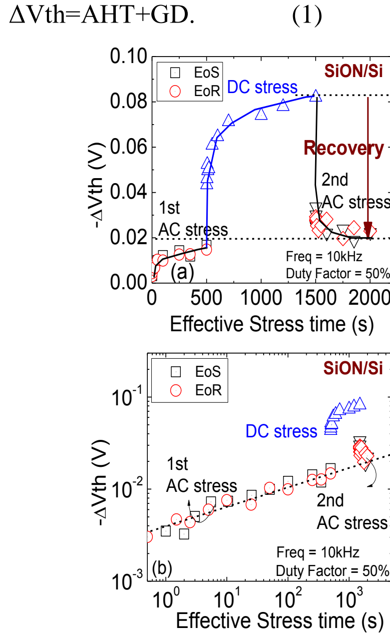

Fig. 2 In SiON/Si device, (a) The DC-enhanced charging recovers during 2nd AC stress. (b) The AC-DC-AC stress follows the same generation kinetics [5].

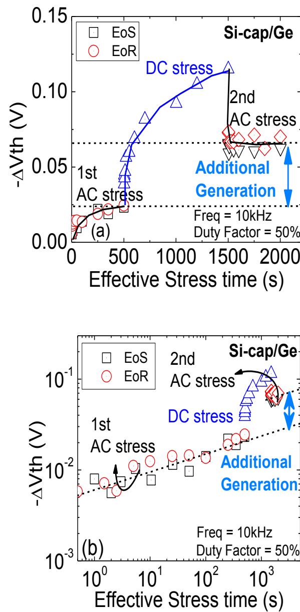

Fig. 3 In Ge devices, (a) The 2nd AC stress cannot fully recover the DC-enhanced NBTI (b) AC-DC-AC stress does not follow the same generation kinetics [5].

AHTs are located below the top edge of Si valence band, Ev, as shown in Fig. 4a. They are charged up under DC stresses, but neutralized under Vg=0, and dominates the recovery when switched to AC stress in Fig. 2.

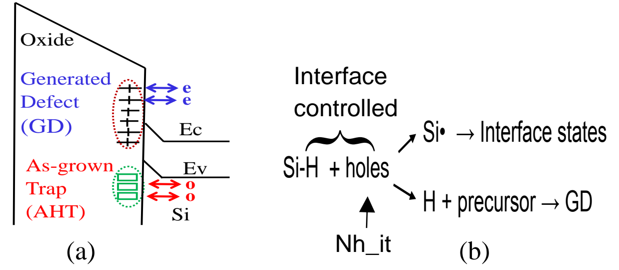

Fig. 4 SiON/Si: (a) AG model and (b) Interface controlled generation: Interface states and GD are two products of the same controlling reaction.

On the other hand, GDs have higher energy level, are more difficult to neutralize, and dominate the NBTI under AC stress. Fig. 2 indicates that the generation process is controlled by the accumulative time under a stress bias, Vgst. The interruptions of Vgst during AC stress have little effects on GDs. It has been reported that for every generated defect in gate dielectric, there is a generated interface states [9]. We speculate that the GDs in dielectrics and the created interface states are the two products originating from the same controlling electrochemical reaction at the SiON/Si interface, as illustrated in Fig. 4b. It is possible that the reaction starts from breaking a Si-H bond at the interface and the breaking rate depends on the oxide field and hole density at the interface, Nh_it. For both DC and AC stresses, the same Vgst gives the same Nh_it, and in turn the same GD in Fig. 2. In this way, one may call the generation in Si device as 'interface-controlled'.

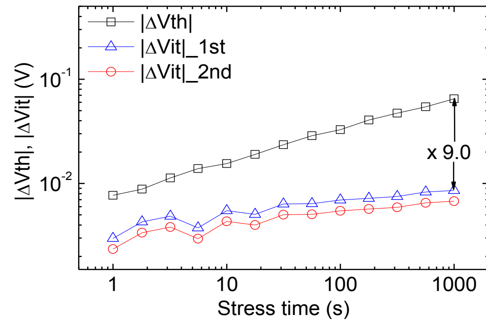

Fig. 5 Ge devices: A comparison of the shift induced by generated interface states, ΔVit, with the total ΔVth [3].

For Ge devices, there are also AHTs and they dominate the recovery in Fig. 3, similarly to the AHTs in SiON/Si devices. The differences in Ge and SiON/Si devices are mainly in the GDs, which are responsible for the 'additional generation' marked out in Fig. 3. Unlike

SiON/Si devices, there is no one-to-one correlation between GD in dielectric and created interface states and Fig. 5 shows that the GDs in dielectric can be substantially higher than the generated interface states.

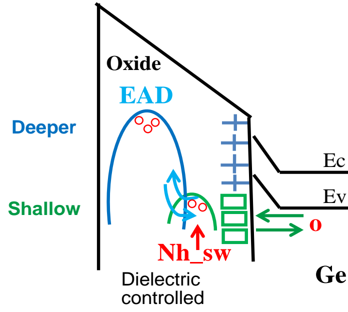

Fig. 6 Ge devices: Dielectric-controlled two-step generation: holes are captured by shallow well and then move to deep well through relaxation. The energy level alters with charge status.

We propose that the generation in Ge is a 'dielectric-controlled' process. It has two steps. In the first step, a defect in the dielectric captures a hole into a shallow well from substrate. This initiates a structure relaxation process, which ends when the captured hole overcomes a barrier and trapped stably in a deeper well, as illustrated in Fig. 6. The generation rate here is controlled by the number of holes in the shallow well of the dielectric, Nh_sw, rather than at the interface. Under AC stress, Nh_sw can be lower than that under DC stress, since the holes in the shallow well is not stable and can tunnel back to the substrate during the Vg=0 phase of the AC stress. As a result, the DC stress induced 'additional generation' in Fig. 3 can originate from the higher Nh_sw under DC stress. The generation in Ge devices is a 'dielectric-controlled' relaxation process [5].

The physical process described above for Ge devices involves the defect energy alternation during the generation process: the neutral precursor has a shallow well, but the charged GD settles down in a deeper well [3]. To support such energy alternating defects (EADs) indeed existing in Ge devices, we compare the discharge-then-recharge of GDs in Ge and SiON/Si devices.

In Fig. 7a, we first charged up the defects by stress. They were then progressively discharged by sweeping Vg in steps in the positive direction. This is followed by a recharge, where Vg was swept back towards negative [2,10,11]. For the SiON/Si devices, it can be seen that the difference between the recharge and discharge is small, indicating that the energy level of the GD changes little after discharge, so that the defect can be recharged as it moves above Fermi level again. For fresh SiON/Si, there is little defects above Ev(Si) [10,11]. The presence of defects above Si(Ev) after stress indicates that a neutralized GD does not return to its precursor state.

Fig. 7b shows that the Ge device behaves differently: when Vg and (Ef-Ef_FB) was swept toward negative direction, there is little recharge until Ev(Ge) was reached. This is because neutralizing a defect alters its energy level back to the shallow well at ~Ev(Ge), so that they cannot be recharged until reaching Ev(Ge). In another word, the energy level of EADs in Ge alters with their charge status: shallow when neutral and deeper when charged. A neutralized GD can be reset to its original precursor statue, therefore.

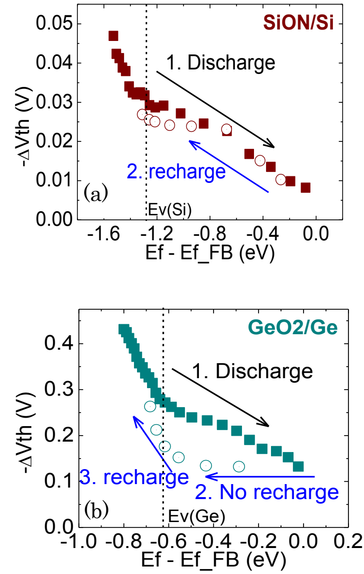

Fig. 7 Differences in defects: (a) Recharge starts as soon as energy sweeping negatively, well above ~Ev(Si) for SiON/Si. (b) Recharge is negligible when biased above ~Ev(Ge) for GeO_2/Ge [5].

IMPACT ON LIFETIME PREDICTION

According to the As-grown-Generation (AG) model, the AHTs typically saturate in seconds and only the GD component follows the power law [10,11]. For silicon devices, AHTs contribution is insignificant under AC stress [10,11], as they are efficiently neutralized during the Vg=0 phase. Under DC stress, AHTs can also be effectively neutralized if there is a measurement delay of ~10 ms [9,12]. Fig. 8a shows that the DC NBTI with a delay can be used as an approximation of AC NBTI. As a result, the lifetime of AC NBTI can be estimated from the DC NBTI with a measurement delay, as shown in Fig. 8b.

Although AG model is also applicable to Ge devices and the AHTs are efficiently neutralized for DC stress with a measurement delay, the DC NBTI with a delay should not be used for estimating the lifetime of AC NBTI, since the dielectric-controlled generation of energy alternating defects (EADs) introduces an additional generation under DC stress, as shown in Figs. 3 and 9a. Fig. 9b shows that the use of DC NBTI even after a delay

will underestimate the AC device lifetime of Ge.

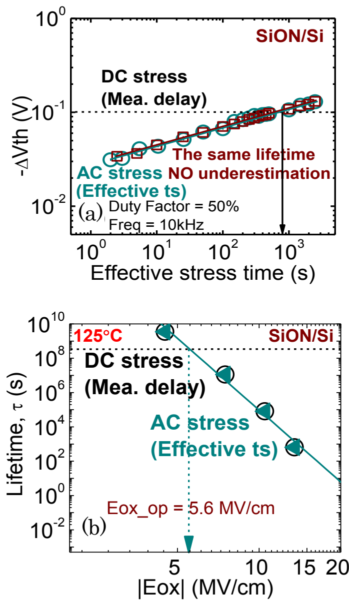

Fig. 8 SiON/Si: A comparison of AC and DC stress with a measurement delay (a) kinetics and (b) lifetime [5].

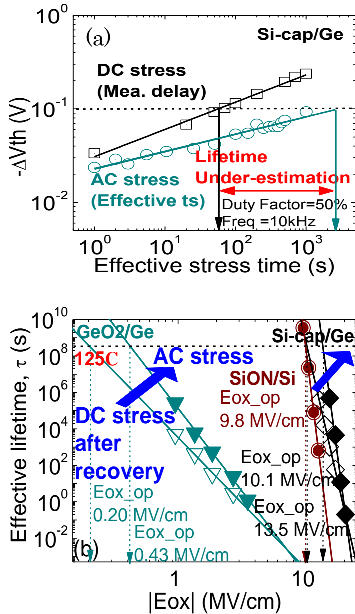

Fig. 9 Ge devices: A comparison of AC and DC stress with a measurement delay (a) kinetics and (b) lifetime [5].

CONCLUSIONS

In this work, we reviewed the recent progresses in understanding the NBTI defects in Ge devices and compared them with those in Si devices. Both Si and Ge devices follow the As-grown-Generation (AG) model. The GDs in SiON/Si devices are interface-controlled, similar under DC and AC stresses, their energy level change little with their charge status, and they do not return to their original precursor state after neutralization. In contrast, GDs in Ge devices are dielectric-controlled, with additional generation under DC, their energy level alternates with their charge status, and they can be reset to their precursor state following neutralization. As a result, DC stress will substantially underestimate the AC lifetime of Ge devices even after a measurement delay and must not be used.

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