Origins and Implications of Increased Channel Hot Carrier Variability in nFinFETs

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Of the MOSFET degradation mechanisms, the variability of Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature Instability (BTI) in deeply scaled devices has been described with a degree of success [1,2]. In comparison to these cases, Channel Hot Carrier (CHC) degradation is inherently more complex [3,4]. CHC stress is non-uniform, with large currents present, and the resulting degradation is typically localized at the drain, thus offering a wider range of variability sources, as well as potential measurement artifacts. Variability of CHC degradation has been reported previously, mainly in planar devices [5-9]. Here we reexamine this topic in two generations of nFinFET devices and observe that *CHC variability is generally higher than that of BTI*, *flagging it as the main contributor to time-dependent variability of FinFETs* [10]. We examine in detail several *intrinsic* (random) and *extrinsic* (process-induced, systematic) sources of this increased variability. To aid this procedure, we demonstrate that *matching pairs* [7] *can be used to eliminate extrinsic (process-related) time-dependent variability sources,* analogously to time-0 variation [11]. We discuss *the intrinsic variability sources in the defect centric framework* [2,12] and *provide a blueprint for projecting CHC variability to operating conditions and lifetimes.*

A population of nFinFET devices with (as drawn) gate lengths L_G ranging from 130 nm down to 28 nm, fin height ~30 nm, high-k gates, fabricated in two imec technologies, distributed across wafer, have been subjected to either CHC or PBTI stress at either RT or 125 °C. An example of the increased spread of CHC degradation wrt BTI for the same mean threshold voltage shift $\langle\Delta V_{th}\rangle$ is in Fig. 1. In the following we quantify the variability in terms of average charged trap impact $\eta = \sigma_{\Delta Vth}^2/(2\langle\Delta V_{th}\rangle)$ (eq. 1), a crucial defect-centric parameter [2,13]. We first identify several potential sources of this increased CHC variability (Fig. 2). Since the CHC energy distribution is an intricate function of the electric field distribution in the device body, a dependence on device length (Fig. 2a) and biases (Fig. 2b) variations can be expected. From CHC $\langle\Delta V_{th}\rangle$ vs L_g dependence (not shown) we can readily extract the effect's sensitivity to channel L_g variation to be (technology dependent) ~2.5 mV/nm. With this in mind and assuming σ_{Leff} = 2 nm, η = 0.13 mV (cf. Eq. 1), suggesting this mechanism is not the main contributor to CHC variability. Fig. 3 illustrates the sensitivity of CHC energy distribution at the drain to the drain bias V_D. Again from measurements of CHC $\langle\Delta V_{th}\rangle$ vs. V_D (not shown) we can conclude that η is negligible 0.07 mV for σ_{VD} = 10 mV, however, η is considerable 2.2 mV for σ_{VD} = 50 mV. Setting aside circuit implications of varying V_D for the moment, we conclude that variations in source/drain series resistance (Fig. 2b) could be responsible for the increased CHC variability. We, however, observe no correlation between channel current during CHC stress and the resulting ΔV_{th} (Fig. 4), as well as similar variability (η) when CHC is applied with equivalent constant drain *current* (not shown), eliminating this extrinsic source of variability as well.

To resolve the general issue of extrinsic (artefact) variability sources, we introduce matching pairs (MP) [7] as a means of eliminating extrinsic (process-related) time-dependent variability sources, analogously to time-0 variation [11]. In Fig. 5 we illustrate that *the correct (intrinsic) η can be extracted from the distribution of* $\delta\Delta V_{th} = \Delta V_{th,L} - \Delta V_{th,R}$, i.e., the difference in *degradation* in Left and Right FinFETs of each MP, *even if across-wafer process-induced variability is assumed.*

The method is first applied to long, 1st-generation imec FinFETs. Fig. 6 confirms that CHC variability is generally higher than that of BTI. We see that η extracted after BTI stress scales as device area A^{-1}, as expected for defects distributed uniformly over the channel [14]. On the other hand, the larger CHC variability is ~constant and ~merging with the BTI trend at shorter gate lengths. This trend can be traced to the CHC degradation localized at the drain (cf. Fig. 2c). As documented in Fig. 7, CHC degradation is asymmetric down to L_g = 45 nm (technology dependent), coinciding with CHC simulations at $V_G = V_D$, indicating maximum damage ~20 nm from the drain junction into the channel (not shown). The CHC vs BTI trend of Fig. 6 is then qualitatively well reproduced by TCAD simulations [15], see Fig. 8, with uniform (BTI) and localized (20 nm from the drain) trapped charge in the nFinFET gate oxide, confirming longitudinal localization of damage (Fig. 2c) as a source of increased long-channel nFinFET CHC variability wrt BTI.

Fig. 9 again documents the extraction capability of the MP technique (Fig. 5) for short, 2nd generation devices for both time-0 (Fig. 5a) and time-dependent variability (Figs. 5bc). Again, η after BTI stress scales with A^{-1} (Fig. 5b), while CHC stress again results in higher variability (η). Compared to PBTI, CHC stress is known to result in significant Si interface defect generation (e.g., ~2.2×10^{11} cm^{-2} from Charge Pumping on large-area devices of 1st generation FinFETs at applied stress conditions), typically accompanied by a subthreshold slope increase. We conclude that charged defects generated close to/at the substrate [16] (cf. Fig. 2d) are the main source of the increased CHC variability in short nFinFET devices. This is also evidenced by TDDS measurements [11] on pristine and previously stressed devices, showing for CHC stress *a high-η mode corresponding to defects close to the Si interface* (Fig. 10) [16,17].

Based on the above discussion including careful elimination of potential variability artefacts, we conclude that the total CHC nFinFET distribution will be bimodal, pertaining to bulk charging and to interface defect generation, respectively (Fig. 11). Note that the interface defect mode may not be quantifiable in small populations of devices and for short stress times. Both modes will need to be extracted and their kinetics projected separately toward operating/lifetime conditions. This task will be facilitated by *analytic description of multimodal defect-centric statistics,* as outlined in [18], as well as *the use of matching pairs to correct for extrinsic time-dependent variability sources*.

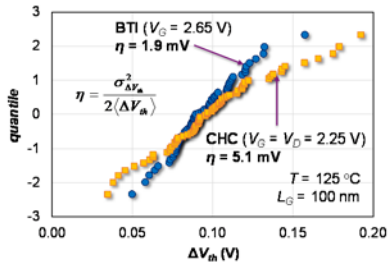

Fig. 1: For the same mean degradation, CHC stress in nFinFETs results in a wider distribution, as compared to uniform BTI stress.

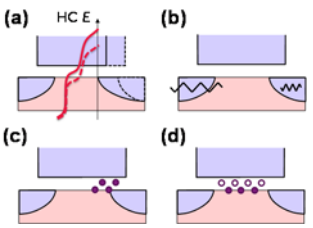

Fig. 2: Sources of increased CHC variability: (a) Channel length/LER and schematic CHC energy distribution, (b) series resistance, (c) longitudinally and (d) vertically non-uniform trapping.

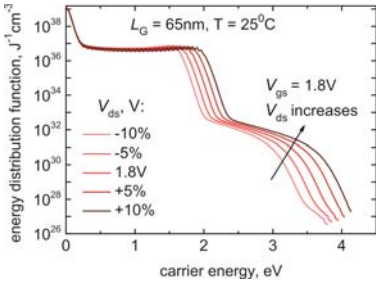

Fig. 3: CHC energy distribution at drain (cf. Fig 2a), responsible for trap generation and charging, is sensitive to drain bias.

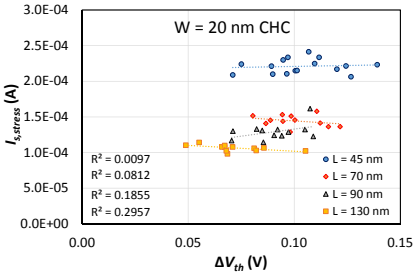

Fig. 4: Channel current during stress is not correlated with degradation, disqualifying series resistance as a main source of increased CHC variability.

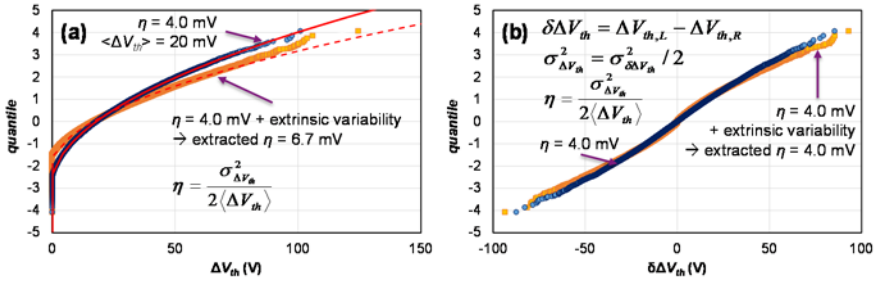

Fig. 5: Probit plots of MC simulation of defect-centric distributions in (a) single devices (SD) and (b) matching pairs (MP). Variance and hence η can be readily extracted from the difference distribution $\delta\Delta V_{th}$ obtained on MPs (b). Note the MP distribution is in general not normal. *Additional extrinsic variability*, generated by distributing defect density N_T, in single devices (a) *is fully compensated and the original η is restored* (b).

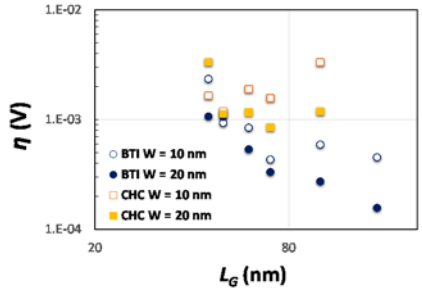

Fig. 6: Gate length dependence of BTI and CHC variability in long nFinFETs, as extracted from MPs (cf. Fig. 5). BTI η dependence follows A^{-1} scaling, while CHC η is higher, approx. constant and hence tends to converge at shorter gate lengths.

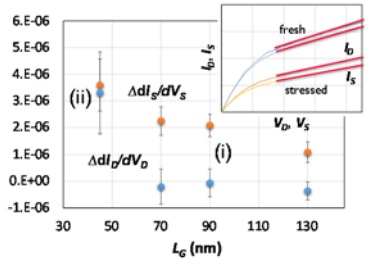

Fig. 7: Change in dI_d/dV_d (dI_s/dV_s) slope after CHC stress (inset) allows visualizing CHC degradation i) longitudinally localized in longer nFinFETs and ii) spanning the entire channel in shorter devices. BTI degradation is symmetric at all L_G's (not shown).

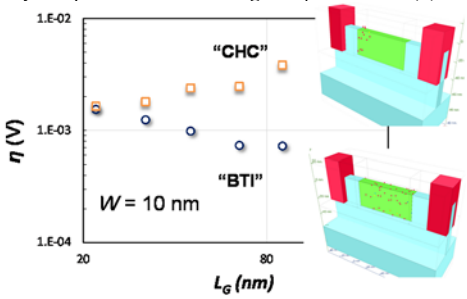

Fig. 8: "Atomistic" TCAD simulation [15] of uniform (BTI) and localized (CHC) degradation in *synthetic* nFinFETs (inset) qualitatively well reproduces measured dependence (open symbols) in Fig. 6.

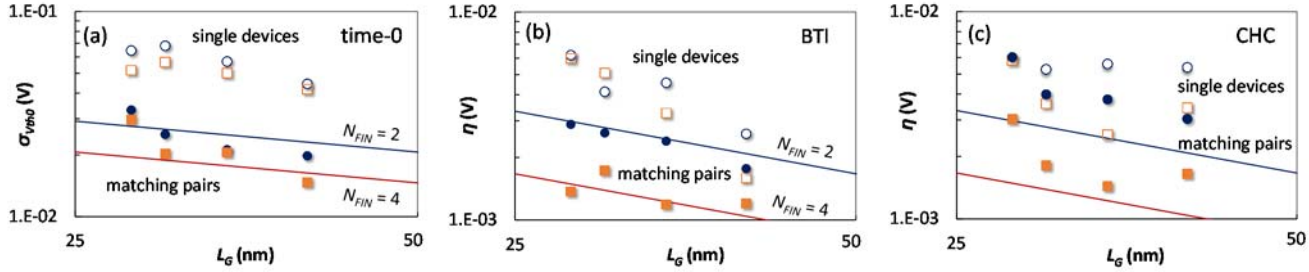

Fig. 9: (a) *Time-0* variability, represented by σ_{Vth0}, and *time-dependent* variability after (b) BTI and (c) CHC stress, as extracted from *single* short nFinFETs (SD, open symbols) and from *matching pairs* (MP, solid symbols). Unlike SDs, MPs yield correct area scaling for both time-0 (lines: $\sigma_{Vth0} \sim Area^{-1/2}$) and BTI (lines: $\eta \sim Area^{-1}$, cf. Fig. 6). CHC stress (c) results in higher variability wrt BTI [fit lines from (b) copied over to (c)] due to defect generation at oxide/substrate (cf. inset of Fig. 11).

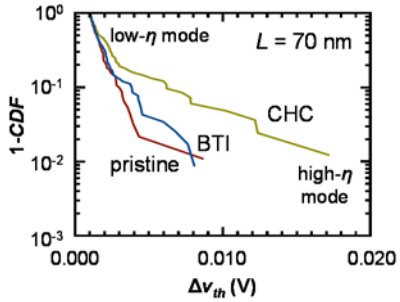

Fig. 10: Single trapping event Δv_{th} distributions obtained from TDDS measurements show increased defect density at close channel/oxide interface (high η; cf. Fig. 2d) after CHC stress.

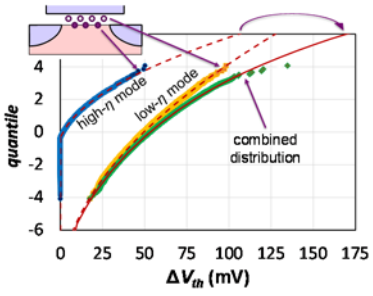

Fig 11: Bimodal defect-centric distribution ΔV_{th} corresponding to CHC stress: MC and analytic fit [18]. The high-σ tail of the full distribution is controlled by defects at the substrate (high η; inset: solid syms).

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