Realization of NOR logic using Cu/ZnO/Pt CBRAM

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Abstract

A method is proposed to realize NOR logic. Unlike existing solutions, the new solution has no requirements on unrealistic device characteristics such as high asymmetry to operating voltages or the small variations. By comprehensive analysis and the fabrication of Cu-based conductive-bridge- RAM, we show the reliably implementation, which paves ways for future low-power reconfigurable computing.

(Keywords: in-memory computing, RRAM, NOR logic)

Introduction

Driven by the demand for high flexibility and in-situ processing in the era of big data, the field-programmable gate arrays (FPGAs) have extended their use from simple prototyping tasks to the reconfigurable computing [1]. Commercial FPGA technology suffers from high power consumption and thus the realization using emerging memory technology to achieve in-memory computing and non-volatile storage simultaneously can be an intriguing solution [2]. Wherein, RRAMs-based solutions have raised great interest due to the simple structure, high density, good scalability, and CMOS compatibility.

FPGA relies on the realization of one fundamental logic, based on which all the Boolean logic can be constructed. Several schemes have been proposed, such as the logic IMPLY using Material Implication [3] and the logic NOR using memristor added logic (MAGIC) [4]. Both schemes are conceptual-intriguing but impossible to be implemented with existing RRAM technologies: 1) It has been pointed out that the IMPLY requires the use of extra resistors, which is hard to match both High Resistance State (HRS) and Low Resistance State (LRS) at the same time [6,7]; 2) For MAGIC (Fig. 1a), it has stringent requirement for V_{SET}/V_{RESET} [8], which most RRAM devices [9–15] cannot satisfy as shown in the inset of Fig. 1(b). Besides, it also suffers the weak tolerance to the resistance variation, as shown in Fig. 1(c).

In this paper, we proposed a new solution to realize logical NOR. A detailed analysis on the requirement for both voltage and resistance are carried out. Based on this, Cu/ZnO/Pt material system is selected to construct the RRAM device, with which we show that NOR can be reliably achieved.

Basic Logic Cell

We define HRS of RRAM as logic 0 and LRS as logic 1. By dividing NOR logic to two steps, we introduce OR and NOT operation, separately.

A. *OR operation*

As shown in Fig. 2(a), the basic cell of OR gate consists of four RRAMs, with two TEs and two BEs on the common line. The left two and right two represent logical inputs and outputs respectively. Logic operation starts by initializing M_1 and M_2 to HRS, then pulse signals with the magnitude of V_o are applied on A and B, while M_1 & M_2 are kept grounded. Four input cases, LL, LH, HL, HH, can be divided into two categories as below:

- If input has at least one LRS, the total resistance for input RRAMs is almost LRS, since HRS can be ignored when parallel connected with LRS. Then V_x is close to V_o, results in voltage drop of V_o on M_1 and M_2, finally SET output RRAMs to LRS.
- If both input RRAMs are HRS, total pull up resistance equals to HRS/2, while total pull down resistance is HRS/2 as well, which means V_x is $V_o/2$. By setting V_o to make $V_o/2<V_{SET}$, then M_1 and M_2 will keep HRS.

Besides, from the state change of different input cases shown in Fig. 2(b), a definition of V_o is determined as:

$$\frac{1}{2}V_o<V_{SET}<V_o \quad (1)$$

Simulation results of 4cases are shown in Fig. 2(c) with each cycle for one input case.

B. *NOT operation*

For NOT operation, the structure is in Fig. 3(a) with BE of two input RRAMs and TE of one output RRAM on the common line. By stressing V_o on BE of M_1 and M_2, and grounding TE of Y, V_x is determined by input resistances. The first step is initializing Y to LRS. If input two RRAMs are with LRS, V_x is $2/3V_o$, which leads to voltage drop of $-2/3V_o$ on Y and $-1/3V_o$ on M_1&M_2. In order to RESET output RRAM to LRS and maintain the state of input RRAMs, V_o should satisfy:

$$\frac{1}{3}V_o<|V_{RESET}|<\frac{2}{3}V_o \quad (2)$$

The correct functionality is confirmed with simulation shown in Fig .3(c). According to Eq. (1) & (2), the

relationship between V_{SET} and V_{RESET} is shown in Fig. 4, which means the harsh requirements of asymmetric switch character for MAGIC NOR gate is avoidable.

Variation Analysis

In practice, the variations in both voltage and resistance are nonnegligible and can affect V_x and in turn the correctness of basic logic. For OR gate, V_x is disturbed only when input case is HH, since in other cases pull up resistance is far less than pull down resistance. With HRS variation σ_H considered, mean value of V_x is $1/2V_o$ and has maximum value $[1/(1-3/2\cdot\sigma_H+1)]\cdot V_o$, which should lower than minimum V_{SET} with variation, $(1-3\sigma_{VSET})\cdot\mu_{VSET}$. Due to OR gate presets V_{SET} in the middle of $1/2V_o$ and V_o to differentiate different input cases, $\mu_{VSET}=3/4V_o$ gives the maximum region for tolerating variation. Conjoint analysis for impact of σ_H and σ_{VSET} on logic correctness is written as Eq. (3), and the curve is shown in Fig. 5(a). With green for tolerable σ and red for failed cases, the area below curve corresponds to σ_H and σ_{VSET} value that can make the logic correct.

$$\sigma_H<\frac{2}{3}\cdot\left[2-\frac{4}{3}\cdot(1-3\cdot\sigma_{VSET})\right] \quad (3)$$

For NOT gate, V_x is disturbed when input two RRAMs are with LRS and the mean value is $2/3V_o$. When considering LRS variation σ_L, V_x has maximum value $[2/(1+3/2\cdot\sigma_L+2)]\cdot V_o$, and it should larger than minimum $|V_{RESET}|$ with variation, $(1+3\sigma_{VRESET})\cdot|\mu_{VRESET}|$. In order to switch output RRAM and leave input RRAMs unchanged, $|\mu_{VRESET}|=1/2V_o$ gives the maximum region for tolerating variation. Conjoint analysis of σ_L and σ_{VRESET} is written as Eq. (4), and the curve is shown in Fig. 5(b). The area below curve represents logical correctness.

$$\sigma_L<\frac{2}{3}\cdot\left(2\cdot\frac{2}{1+3\cdot\sigma_{VRESET}}-3\right) \quad (4)$$

Device Fabrication

We fabricated Cu/ZnO/Pt device with process shown in Fig. 6(a). The I-V curve and device structure are shown in Fig. 6(b) and inset, respectively. As shown, the I-V curve is slightly asymmetric under positive and negative voltage sweep, which is due to the different mechanism of SET and RESET process. By applying a positive voltage to the Cu TE, Cu atoms dissolute and migrate into ZnO film under the applied electric field and eventually leads to a reduction at Pt BE and Cu atoms conductive filament (CF) formed from BE to TE. As a result, a large current flowing through CF immediately reaches the compliance current, and the voltage is V_{SET}. Once the bias polarity is reversed and compliance current removed, Cu CF is broken either by reduction or Joule heating so that low current can flow, corresponding to HRS and the voltage is V_{RESET}. AFM and 3D topographic image of the intrinsic ZnO film is shown in Fig. 6(c).

As shown in Fig. 7, the V_{SET} and V_{RESET} has $\sigma_{VSET}=0.1$ and $\sigma_{VRESET}=0.09$, respectively and the resistance variation σ_H and σ_L are both lower than 0.3. However, due to the variation still fail to meet demands, one solution is proposed to relax this requirement. Unlike the input RRAMs which usually hold intermediate values from previous calculation step, the output RRAM needs to be SET/RESET for OR/NOT gate before logic operation. This allows us to assign relatively accurate value to output RRAM. Assuming u*H is assigned for M_1&M_2 in OR gate, with u decreasing, as shown in Fig. 8(a), the curve of σ_H and σ_{VSET} is uplift, which means larger tolerance. Similarly, assuming s*L is assigned for Y in NOT gate, the tolerance also increases as s increases, as shown in Fig. 8(b). Simulation on logic correctness with parameters from our device is shown in Fig. 9. The device with symmetric switch voltage can realize NOR logic through our method and with precisely control, the correctness comes to 100% even with variation.

Circuit and Performance

To accommodate both basic cells into the standard crossbar structure (Fig.10a), a peripheral circuit is designed and need to be connected in each column (Fig. 10b). The two additional RRAMs is used to hold intermediate output result from OR operation. Sequence of voltage source is shown in Fig. 10c, in which OR, NOT and READ Y is implemented in order. Comparison in steps and RRAM cells for NOT, OR, NOR logic with other methods is shown in Fig .11.

Conclusion

A new solution to achieve NOR logic is proposed using the crossbar structure, which conquered the conventional unrealistic requirement for asymmetric voltage. By further exploring the requirement for the variation of the device characteristics in resistance and switch voltage，we show the solution is possible to be implemented in many existing technologies conquering the unrealistic asymmetric voltage requirement. Finally, we fabricated Cu/ZnO/Pt CBRAM and demonstrate the feasibility of the proposal.

References

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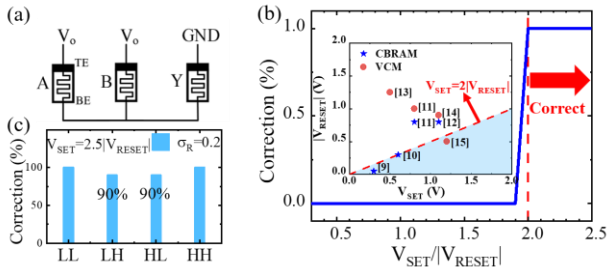

Fig.1 (a) Circuit structure of MAGIC NOR gate. **(b)** Simulation of Correction vs $V_{SET}/|V_{RESET}|$, the inset is distribution of switch voltage of CBRAM and VCM RRAM. **(c)** Simulation with resistance variation σ_R=0.2

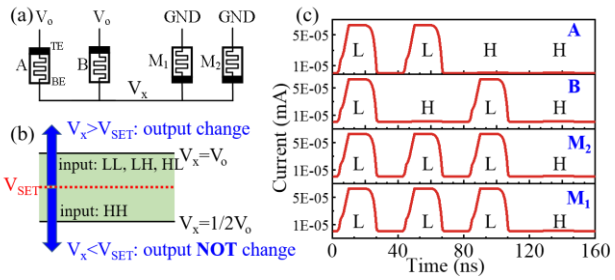

Fig.2 (a) Basic structure of OR gate. **(b)** Voltage requirements and change of state for different input case. **(c)** Waveform for all four input cases and the correct outputs.

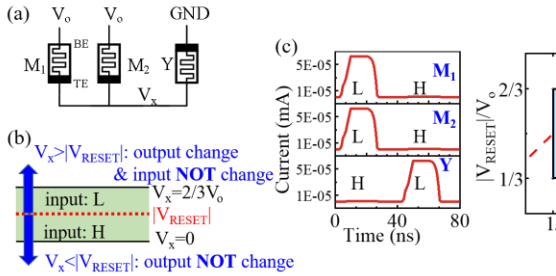

Fig.3 (a) Basic structure of NOT gate. **(b)**Voltage requirements and change of state for different input case. **(c)** The waveform for two possible input cases and the correct outputs.

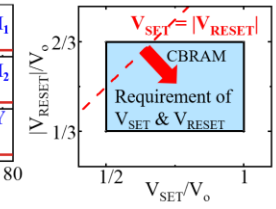

Fig.4 Requirement for device from two steps. Device with symmetric switch voltage can work.

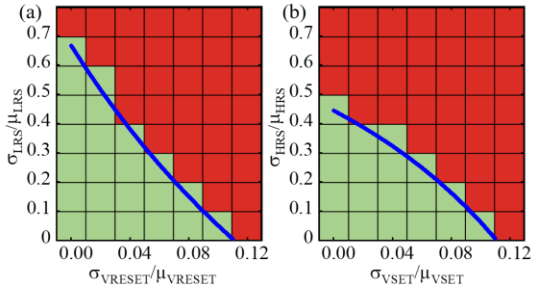

Fig.5 Mapping of successful (in green) and failed (in red) cases for logic cell with different **(a)** σ_H and σ_{VSET}, **(b)** σ_L and σ_{VRESET}. The curve is the boundary of maximum allowable variation.

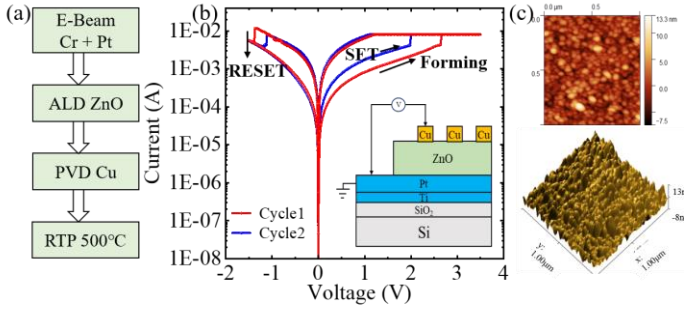

Fig.6 (a) Fabrication process of Cu/ZnO/Pt device. **(b)** Typical IV curve for Forming and second SET/RESET transitions. The inset is the device structure and measurement configuration. **(c)** AFM images of the intrinsic ZnO film and 3D topographic image.

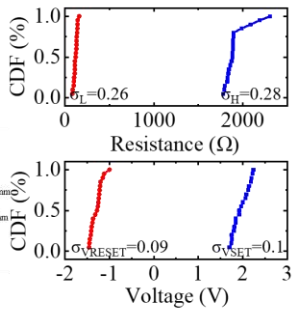

Fig.7 Cumulative distribution for high/ low resistance, V_{SET} and V_{RESET} of fabricated device.

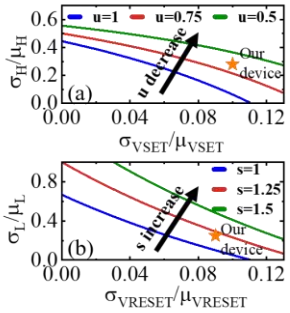

Fig.8 Tolerance changes with different initial value of **(a)** M_1&M_2 =u*H and **(b)** Y =s*L.

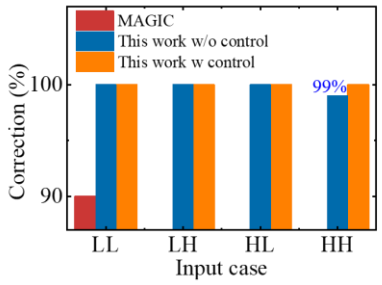

Fig.9 Simulation results based on our device for MAGIC, this work w/o and with precisely control the initial state of output RRAM.

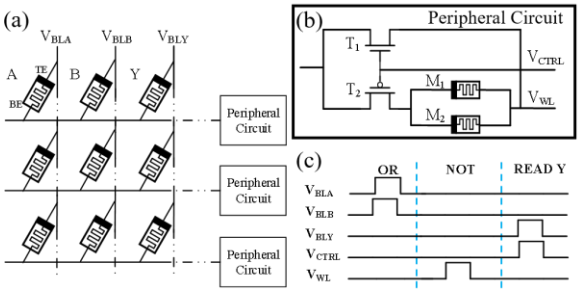

Fig.10 (a) Construction in circuit level. **(b)** Details of peripheral circuit. **(c)** Timing sequence for control and line voltage source to realize NOR logic.

# OF RRAM CELLS/ # OF CYCLES			
Logic	**IMPLY**	**CRS**	**This Work**
NOT	2/1	4/2	1/1
OR	4/3	8/3	2/1
NOR	6/4	12/5	3/2

Table I. Comparison in steps and RRAM cells for NOT, OR, NOR logic with other methods.