A Space Vector PWM with Common-Mode Voltage Elimination for Open-End Winding Five-Phase Drives with a Single DC Supply

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***Abstract*–Open-end winding three-phase drive topologies have been extensively investigated in the last two decades. In majority of cases supply of the inverters at the two sides of the winding is provided from isolated dc sources. Recently, studies related to multiphase open-end winding drives have also been conducted, using isolated dc sources at the two winding sides. This paper investigates for the first time a five-phase open-end winding configuration, which is obtained by connecting a two-level five-phase inverter at each side of the stator winding, with both inverters supplied from a common dc source. In such a configuration it is essential to eliminate the common-mode voltage (CMV) that is inevitably created by usual PWM techniques. Based on the vector space decomposition (VSD), the switching states that create zero CMV are indentified and plotted. A space vector pattern with large redundancy of switching states is obtained. Suitable space vectors are then selected to realize the required voltage reference at the machine terminals with zero CMV. The large number of redundant states enables some freedom in the choice of switching states to impress these space vectors. Out of numerous possibilities, two particular switching sequences are chosen for further investigation. Both are implemented in an experimental set-up, and the results are presented and discussed.**

***Index Terms*–Multiphase drives, open-end winding, pulse width modulation, induction motor drives.**

I. Introduction

Multiphase machines are nowadays recognized as a potentially viable solution for a wide range of applications. A comprehensive review of the state-of-the-art in the area and the advantages offered by such solutions is provided in [1, 2]. Current interest in these drives is mostly the consequence of their better fault tolerance and lower power (current) per-phase rating, when compared to an equivalent three-phase system.

The open-end stator winding topology with power electronic converters connected to both sides of the winding is a supply option which has been investigated extensively in conjunction with three-phase drives. However, the extent to which this option has been considered in relation to multiphase drives is very limited. In [3] the open-end topology was used for an asymmetrical six-phase induction machine in order to achieve harmonic filtering. An asymmetrical six-phase machine was also the subject of [4], where four isolated dc supplies were utilized in order to reduce the system PWM control to the well-known 'nearest three vector' method, customarily used in three-level three-phase neutral point clamped (NPC) voltage source inverters (VSIs). Multiphase open-end winding topology with dual inverter supply has been further considered in [5-7], where space-vector and carrier-based PWM techniques have been developed for five-phase systems.

The common feature of [3-7] is that isolated dc sources are used to supply VSIs at two sides of the multiphase machine's winding. A drawback of the requirement for isolated dc sources is that one or more isolation transformers are required in all applications where separate dc sources do not exist naturally (the requirement for isolated dc sources can be easily met in autonomous power systems that exist in, for example, ships, aircraft, and electric vehicles). Zero-sequence current cannot flow when CMV has non-zero value due to the dc supply isolation, so that the dual inverter supply can provide performance equivalent to multi-level single-sided supply.

In contrast to the existing body of work [3-7], this paper considers a dual two-level inverter supplied five-phase motor drive where a single dc bus is used to supply both inverters. Such a possibility has only ever been considered in conjunction with the three-phase configuration. A further advantage of this topology, in addition to the fact that only a single dc source is required, is that each stator phase is connected in effect to an H-bridge, leading to the doubling of the amount of voltage available at the output. This is indeed perceived as the most favorable feature of this topology since it means that, for a given motor rated voltage, dc bus voltage has to be just over 50% of the value which would have been required in single-sided supply mode with, say, a three-level NPC VSI. This supply option is therefore well suited to general industrial applications which require, in addition to fault tolerance and high output voltage waveform quality, supply of a machine from a dc source of rather low voltage.

However, due to the system configuration, there is now a path for zero-sequence current to flow freely. The CMV, which exists between the two dc buses in the isolated dc source version of the topology, will now lead to a considerable zero-sequence current. Since this current is by

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definition identical in all the phases of the machine, it only produces losses; hence its cause, the CMV, has to be eliminated. The paper builds on the initial considerations of this topology, reported in [8]. However, instead of extensive simulations and initial experiments on a five-phase *R-L* load, the emphasis is here on detailed experimental study using a five-phase induction machine. Since the zero-sequence current is not completely eliminated, regardless of the use of the space vector PWM that should theoretically give zero CMV, a detailed analysis of the sources of the zero-sequence current flow is also provided.

Various approaches have been adopted to achieve CMV and zero-sequence current elimination in three-phase drives with open-end winding configuration. The approach in [9] uses space vectors which do not generate the CMV. Therefore, theoretically, every modulation technique that utilizes only these space vectors would result in zero CMV. This idea, developed for the dual two-level three-phase VSI supply, was later applied in conjunction with various multi-level inverter topologies at the two sides of the stator winding [10-12]. This paper follows the approach adopted in [9] for three-phase drives and extends it to a five-phase open-end topology with dual two-level inverter supply. The switching states giving zero CMV are indentified and the resulting space vector pattern is plotted. The most appropriate space vectors are selected to realize the reference voltage across the machine terminals. It is observed that the space vectors have considerable redundancies. Therefore, two alternative approaches have been adopted to select the appropriate switching states, while applying the same space vectors. The dwell times of these space vectors are derived from a simple carrier-based sinusoidal PWM modulation.

II. Multiphase Open-End Winding Topology with Dual Inverter Supply and Single DC Bus

A schematic of the considered topology is shown in Fig. 1 for a machine with *n* phases. The dc bus voltage V_{dc} (set here to 300 V) is applied to both inverters by connecting their positive (*P*) and negative (*N*) rails. The two inverters (VSI*a* and VSI*b*) have their corresponding switches denoted in Fig. 1 with index *a* or *b* in addition to the machine phase number. The phase voltage references are sinusoidal signals since the machine is with near-sinusoidal spatial m.m.f. distribution.

The topology of Fig. 1 makes it possible to consider each phase as being supplied by an independent H-bridge which can create three voltage levels at the output: $+V_{dc}$, 0 and $-V_{dc}$. Thus, the sinusoidal reference with magnitude of V_{dc} is easily achievable with this topology. The $+V_{dc}$ voltage results by connecting the left-hand end of the stator phase to the positive rail and the right-hand end to the negative rail. The $-V_{dc}$ level is obtained by reversing the connections. However, the zero voltage state can be achieved in two different ways: by connecting both ends to the positive or to the negative rail. In terms of switching states, if the connection to the positive rail is denoted with 1 and to the negative with 0, and the states of the two inverters are separated by a hyphen, these states can be described as 1-0 for $+V_{dc}$, 0-1 for $-V_{dc}$ and 1-1, 0-0 for zero state. The relationship between the two leg voltages and load phase voltage for this topology is, for any phase, given with:

$$v_{phi} = v_{lai} - v_{lbi} \qquad i = 1,2..5 \tag{1}$$

The considerations above are valid for individual phases. However, the study for the complete topology cannot be carried out based on the individual H-bridges, since the elimination of the CMV and zero-sequence current demand a simultaneous analysis of all the phases.

A difficulty imposed by the five-phase topology is that five (instead of three) voltages have to be controlled. The five phase voltages can be transformed into two planes (α-β and *x*-*y* plane) and the zero-sequence component (i.e. CMV). Space vectors of phase voltages in the two planes are given with:

$$\begin{aligned} \underline{v}_{\alpha-\beta} &= (2/5)\left(v_{ph1} + \underline{a}v_{ph2} + \underline{a}^2 v_{ph3} + \underline{a}^3 v_{ph4} + \underline{a}^4 v_{ph5}\right) \\ \underline{v}_{x-y} &= (2/5)\left(v_{ph1} + \underline{a}^2 v_{ph2} + \underline{a}^4 v_{ph3} + \underline{a}^6 v_{ph4} + \underline{a}^8 v_{ph5}\right) \end{aligned} \tag{2}$$

where $\underline{a} = \exp(j2\pi/5)$. The CMV equals the difference of the CMVs of the two inverters and has to be zeroed:

$$\begin{aligned} V_{CM} &= V_{CMa} - V_{CMb} = \frac{1}{5}\sum_{i=1}^{5} v_{lai} - \frac{1}{5}\sum_{i=1}^{5} v_{lbi} = 0 \\ &\sum_{i=1}^{5} s_{lai} - \sum_{i=1}^{5} s_{lbi} = 0 \end{aligned} \tag{3}$$

The condition that the total CMV equals zero is therefore equivalent to having the same number of 'ones' in the selected switching states (labelled *s*) of the two inverters.

The number of switching states can be calculated as follows: both inverters have one switching state with five zeros and one with five ones, five switching states with a single one, five with four ones, ten switching states with two ones and ten with three ones. Switching states from the same group have to be applied from both sides. This gives a total of 252 switching states.

The pattern of the space vectors of the open-end topology that do not create CMV was generated according to equations (1) and (2) and is depicted in Fig. 2. The space vector pattern is the same in both planes, with five different magnitudes of the active space vectors, which form five decagons. Four decagons have parallel sides, while one is shifted by 18 degrees. The relationship between the space vectors in the two planes is as follows: out of the four concentric decagons, the vertices of the outer-most and the inner-most decagon change places and the two middle decagons also change

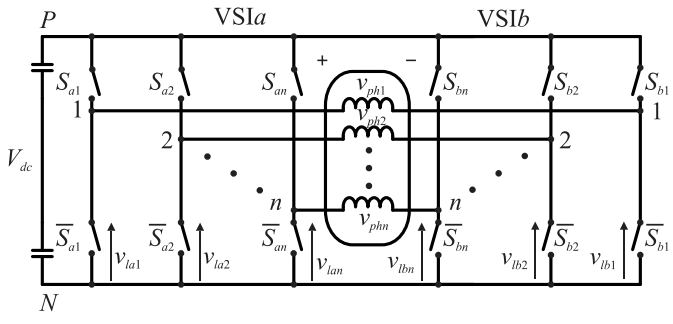

Fig. 1. Open-end winding *n*-phase topology with dual two-level inverter supply and a single dc source.

places. The fifth (shifted) decagon remains the same in both planes. Naturally, the angular positions of the particular space vectors in the two planes are different.

III. Developed Modulation Techniques

A. General Considerations

For the sake of a more detailed explanation of the relationship between the switching states and space vectors, Fig. 3 depicts the part of the space vector pattern that applies to what is referred to here as the first sector. The positions of the sectors are such that they are shifted by 18 degrees clockwise from the sectors of the five-phase single inverter topology. The zero vector has 32 possible switching states, since it can be achieved by applying each of the possible 32 switching states of one inverter at both sides of the winding. Since the two largest decagons in the α-β plane map into the two smallest decagons in the x-y plane and since one wants to achieve zero average voltage in the x-y plane in addition to the zero CMV, the vectors of the outer two decagons of the α-β plane are selected to generate the reference voltages. In a five-phase system one needs to apply five space vectors in a switching period [1] in order to control both planes. These five vectors consist of the zero vector and four active vectors, as depicted in Fig. 2 for the first sector. This sector represents the focus of the explanations in the paper further on, and it is also shown in Figs. 3 and 4. The vectors can be applied in a different order. Two of the possibilities are depicted in Fig. 4 and they relate to the use of pairs of vectors from the two outer-most decagons. The arrangement denoted with solid arrows in Fig. 4 will be explored further in this paper.

Although the sectors are shifted by 18 degrees, there is a strong correlation with the space vectors of the five-phase two-level topology. The magnitudes of the space vectors used here can be expressed as $4/5\cos(\pi/10)V_{dc}$ and $8/5\cos(\pi/5)\cos(\pi/10)V_{dc}$, while the ones used in a single-sided two-level topology with twice higher dc bus voltage can be expressed as $4/5V_{dc}$ and $4/5\cos(\pi/10)/\sin(\pi/5)V_{dc}$. It can be noticed that the ratio of the larger to smaller vector is in both configurations $2\cos(\pi/5)$, and, since the sectors in each case are of 36° span, it can be said that the switching trajectories that the space vector projections make in the two topologies are similar. The space vectors of the open-end topology are $\cos(\pi/10)=0.951$ times smaller than those obtainable in the standard two-level VSI.

There are many possibilities to choose the specific switching states to realize the same vectors. There are 32 switching states for the zero vector, eight for each medium and two for each large vector (Fig. 3). It is essential that the selection of the switching states is done in a manner that imposes the minimum number of switchings when the transfer is made from one vector to another. From (3) it is clear that zero instantaneous CMV can be obtained in two ways. One way is to keep the sum of the switching states the same at each side, which means that the amount of ones in the switching states has to be always the same for two inverters in any time instant. The other way is to keep the difference of the two sums equal to zero by having always the same increment (or decrement) in both sums, so that changes in the individual CMVs of the two inverters take place simultaneously.

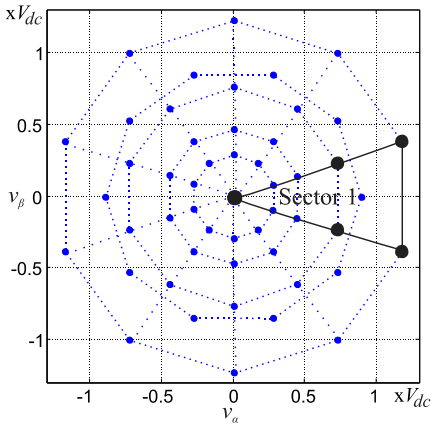

Fig. 2. Space vectors created by switching states that yield zero common-mode voltage (in α-β plane).

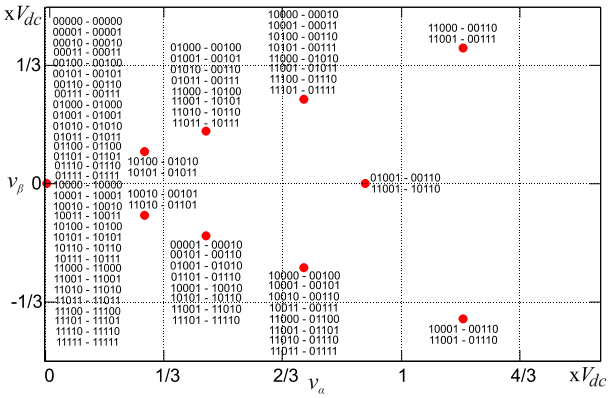

Fig. 3. Distribution of the space vectors and switching states in the first sector of Fig. 2 (in α-β plane).

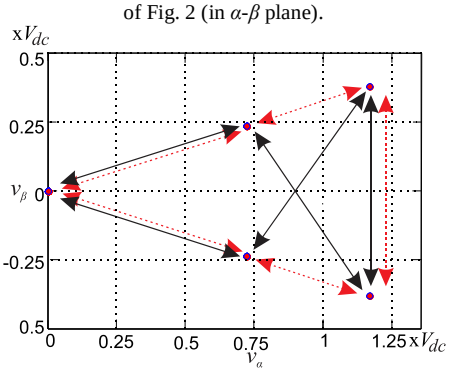

Fig. 4. Two possible arrangements for the application sequence of the selected space vectors (in α-β plane).

Both alternatives require a minimum of two changes in the switching states when a transfer is made from the location of one space vector to the other. In the former case, assuming that one inverter stays in the previous switching state while the other changes the state, the leg that was on has to be switched off and the new one has to be switched on, to keep the amount of legs in state 'one' the same. The latter possibility implies simultaneous state changes in both inverters. If one inverter changes the number of active legs, the other inverter has to follow, to keep the total CMV equal to zero. Obviously, at least two simultaneous changes have to be made in both cases. As a consequence, the inductive load

currents can cause multiple unintended clamping during the dead time, which can lead to low-order harmonics in the voltage waveforms. Some of these harmonics will inevitably map into the CMV. Detailed analysis of the dead-time effect is available in [13] for the three-phase case.

B. Selected Switching Sequences and Implementation

One of the possible switching sequences, selected to comply with the rules of the second alternative and which follows the trajectory described by the solid arrows in Fig. 4, is given with:

$$\begin{aligned} &s_{a1}=[0,0,0,0,0],\ s_{b1}=[0,0,0,0,0]\\ &s_{a2}=[1,0,0,0,0],\ s_{b2}=[0,0,0,1,0]\\ &s_{a3}=[1,0,0,0,1],\ s_{b3}=[0,0,1,1,0]\\ &s_{a4}=[1,1,0,0,1],\ s_{b4}=[0,0,1,1,1]\\ &s_{a5}=[1,1,0,1,1],\ s_{b5}=[0,1,1,1,1]\\ &s_{a6}=[1,1,1,1,1],\ s_{b6}=[1,1,1,1,1] \end{aligned} \quad (4)$$

where the switching states are again denoted with *s*. The subscripts identify to which inverter the switching state applies to (*a* or *b*) and the order of application in a switching period (1…6). This order of switching states is termed 'Sequence 1'. The vectors applied by the individual inverters are shown in Fig. 5 (the large and medium vectors).

The space vectors applied by VSI*a* are the same as those applied by the two-level space vector PWM in the tenth sector in the single-sided supply mode. They are highlighted in Fig. 5. It can be seen from (4) that the switching states applied by the second inverter can be obtained by shifting the first inverter switching states by two to the left. This is equivalent to a shift by $-4\pi/5$ in the α-β plane. Therefore, these space vectors are in fact those that are applied by the two-level space vector PWM in single-sided supply mode in the sixth sector, since one sector spans $\pi/5$. The space vectors applied by the VSI*b* are also shown in Fig. 5. The zero vector is applied by both inverters, the underlined vectors by VSI*b* and the non-underlined ones by VSI*a*. The vectors, applied at the same time by the two inverters, are connected with dashed lines, showing the result of their vector subtraction. The resulting vectors are the highlighted ones in Fig. 2.

Previous space vector related considerations enable subsequent simple implementation, using the carrier-based PWM approach. This is the manner in which both simulations and experiments have been conducted. The first inverter is modulated with the standard five-phase sinusoidal signal references; the second inverter is modulated with the same sinusoidal reference signals delayed by four sectors, i.e. by $4\pi/5$. In order to get at the output the same magnitude and phase shift as in the reference, some adjustments have to be made. It is necessary to modulate the first inverter with a signal that has a phase shift decreased by $\pi/10$, to get its reference in the tenth sector; for the second inverter the phase shift has to be decreased by $9\pi/10$ to get its reference in the sixth sector. This applies to the overall reference positioned in the first sector. The magnitudes of the individual references have to be scaled with the factor $0.5/\cos(\pi/10)$ to achieve the total reference. The scaling is needed since the references of the two inverters have to be subtracted and they are not collinear vectors. The individual references with the appropriate phase shift and magnitude alterations, as well as the overall reference, are also illustrated in Fig. 5.

Since the zero instantaneous CMV is ensured by the switching states, min-max (offset) injection is added to the references to increase the maximum modulation index (defined as the peak fundamental phase voltage over dc bus voltage), in the linear modulation region:

$$v_{inj} = -0.5 \cdot (v_{\min} + v_{\max}) \quad (5)$$

This enhances the dc bus voltage utilization by $1/\cos(\pi/10) = 1.051$. As a result, the maximum fundamental is equal to the one obtainable with the two-level topology in single-sided supply mode without min-max injection (i.e. $M_{\max} = 1$). The illustration in Fig. 5 applies to this maximum modulation index value.

Another possibility that is considered, again for the trajectories shown in black in Fig. 4, is when only one of the two possible zero states (say 0-0) is used rather than both. The switching states for this choice are:

$$\begin{aligned} &s_{a1}=[0,0,0,0,0],\ s_{b1}=[0,0,0,0,0]\\ &s_{a2}=[1,0,0,0,0],\ s_{b2}=[0,0,0,1,0]\\ &s_{a3}=[1,0,0,0,1],\ s_{b3}=[0,0,1,1,0]\\ &s_{a4}=[1,1,0,0,0],\ s_{b4}=[0,0,1,1,0]\\ &s_{a5}=[1,0,0,0,0],\ s_{b5}=[0,0,1,0,0]\\ &s_{a6}=[0,0,0,0,0],\ s_{b6}=[0,0,0,0,0] \end{aligned} \quad (6)$$

This ordering of switching states is termed 'Sequence 2'.

In this case, the application times of the space vectors equal the ones from the previous case, and both originate from the two-level five-phase modulation. Therefore, it is necessary to change the modulation only in a sense that different individual space vectors are to be applied. Figure 6 depicts the space vectors applied by the individual inverters for Sequence 2. Their subtraction results in the same overall vectors in the open-end topology as for Sequence 1. The implementation is this time based on the space vector PWM.

Both approaches have the lowest amount of switching state transitions possible and the switchings are equally distributed among all the legs within a fundamental period. When a single switching period is considered, the switching states of the first method distribute the switchings equally while the second method keeps two legs in each inverter clamped. In this way an individual leg can be clamped for half of the fundamental period and switched four times (rather than the usual two times) in the rest of the fundamental period. The

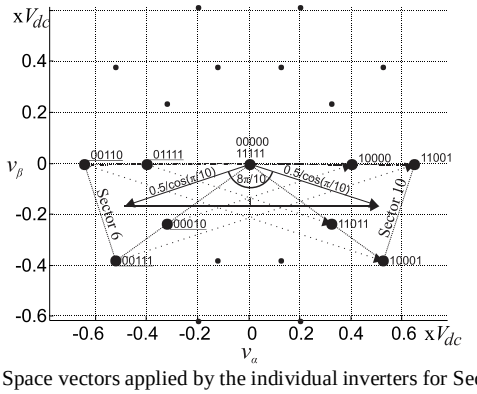

Fig. 5. Space vectors applied by the individual inverters for Sequence 1 when the overall reference is positioned in the first sector (in α-β plane).

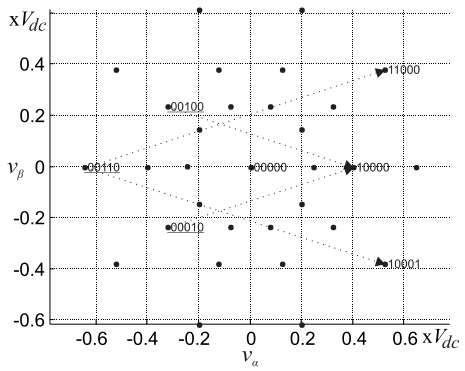

Fig. 6. Space vectors applied by the individual inverters for Sequence 2 when the overall reference is positioned in the first sector (in α-β plane).

techniques apply the same space vectors and produce the same phase voltages; hence the harmonics and THDs are the same. The only differences can occur during the dead time, due to the different switching instants of the semiconductors.

IV. Experimental Verification

The two modulation methods were investigated in detail by simulation in [8]. Hence the emphasis is here on experimental results, so that only a sample of simulation results is given. A five-phase induction machine under no-load conditions is controlled using open-loop *V/f* control without voltage boost. PWM includes the min-max injection and switching frequency is 2 kHz. The inverter dead time is set to 6 µs. The machine parameters are: stator resistance = 3 Ω; rotor resistance = 3 Ω; stator leakage inductance = 45 mH; rotor leakage inductance = 15 mH; magnetising inductance = 515 mH. The number of pole pairs is 2.

The experiments were conducted using two custom-made multiphase two-level inverters connected to a five-phase induction machine. The modulation algorithms have been implemented using a dSPACE DS1006 processor board that provided the gating signals to the inverters via a DS5101 output board. The dc buses of the inverters were fed by a controlled dc supply source, providing a constant 300 V dc bus voltage. The inverters use FS50R12KE3 IGBTs from Eupec (forward voltage drops of the IGBTs and diodes are set to 0.7 V each in simulations, which is the approximate value for the current values encountered here). The phase and leg voltages were measured using high voltage differential probes while the phase current was measured using a current probe. The zero-sequence current was measured by passing both conductors that connect the dc buses through a single current probe. Only the current that flows in the same direction, and thus circulates through the load, was measured in this way. Note that this current is not the zero-sequence component, since it represents each frequency component simultaneously in all five phases. Per-phase values (i.e. zero-sequence components) are therefore 1/5 of the values shown further on.

The experimental results for both sequences are presented in Figs. 7-12 for three values of the modulation index, M = 0.5, 0.8 and 1. Corresponding simulation results for the load phase and leg voltages, for the same conditions, are shown in Fig. 13. As can be seen from experimental and simulation voltage waveforms, the results are in very good agreement.

By comparing experimental results in Figs. 7-12 for the two sequences at the same modulation index values it can be concluded that the phase voltage and phase current waveforms are practically identical. Sequence 1 is however the preferred choice, due to the equalized switching frequency

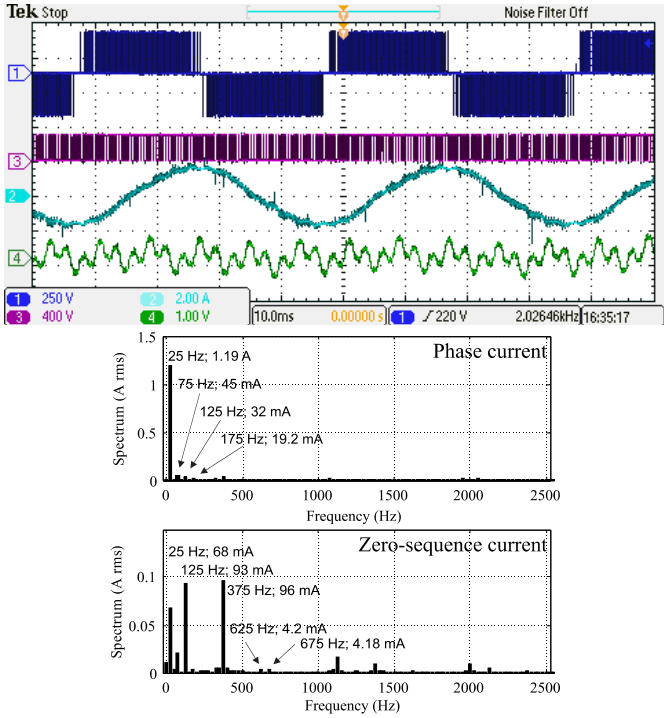

Fig. 7. Experimental results: phase voltage (250V/div), leg voltage (400V/div), phase current (2A/div) with spectrum, and zero-sequence current (1A/div) with spectrum for Sequence 1, M=0.5, f=25 Hz.

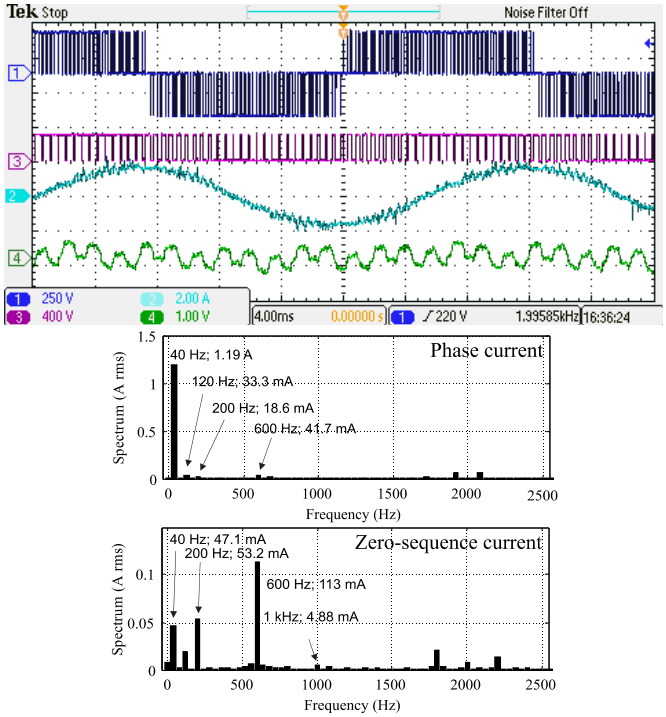

Fig. 8. Experimental results: phase voltage (250V/div), leg voltage (400V/div), phase current (2A/div) with spectrum, and zero-sequence current (1A/div) with spectrum for Sequence 1, M=0.8, f=40 Hz.

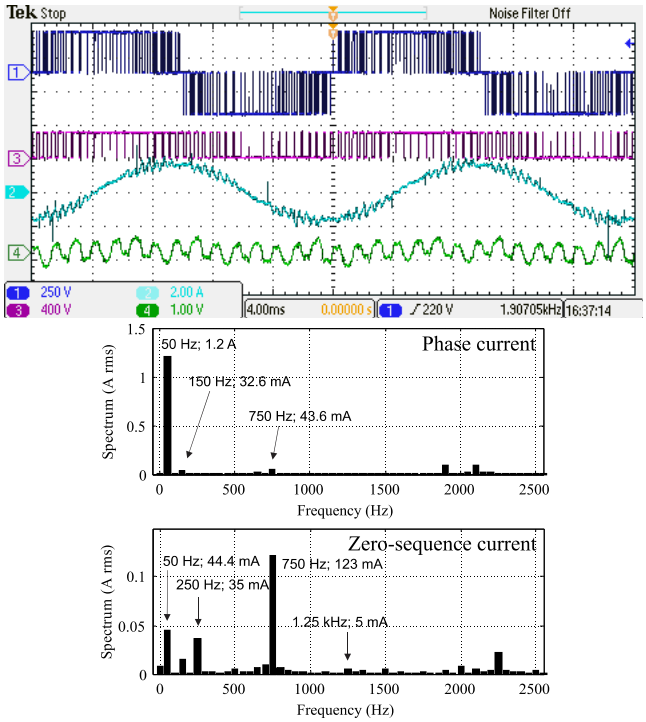

Fig. 9. Experimental results: phase voltage (250V/div), leg voltage (400V/div), phase current (2A/div) with spectrum, and zero-sequence current (1A/div) with spectrum for Sequence 1, M=1, f=50 Hz.

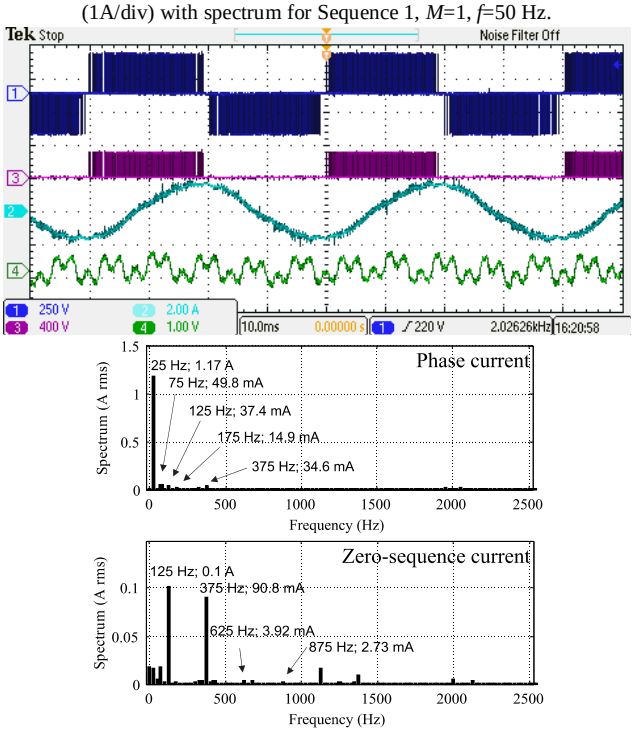

Fig. 10. Experimental results: phase voltage (250V/div), leg voltage (400V/div), phase current (2A/div) with spectrum, and zero-sequence current (1A/div) with spectrum for Sequence 2, M=0.5, f= 25Hz.

in all inverter legs over the entire fundamental period.

The zero-sequence currents are also very similar, containing predominantly harmonics that are multiples of the phase number (i.e. 5), with the fifth and the fifteenth harmonics being the largest.

The experimental and simulation results also show the leg voltages in order to emphasize the difference between the two sequences. It can be seen that Sequence 1 modulates each leg throughout the whole fundamental period at the frequency of 2 kHz. Sequence 2 re-distributes the switchings. In half of the fundamental period one leg of the inverter is clamped while in the other half it switches at double the average switching

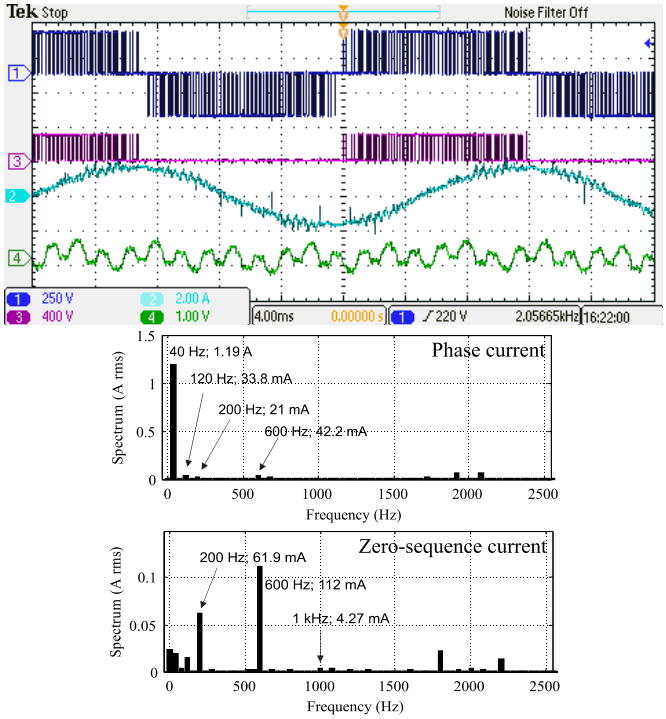

Fig. 11. Experimental results: phase voltage (250V/div), leg voltage (400V/div), phase current (2A/div) with spectrum, and zero-sequence current (1A/div) with spectrum for Sequence 2, M=0.8, f= 40Hz.

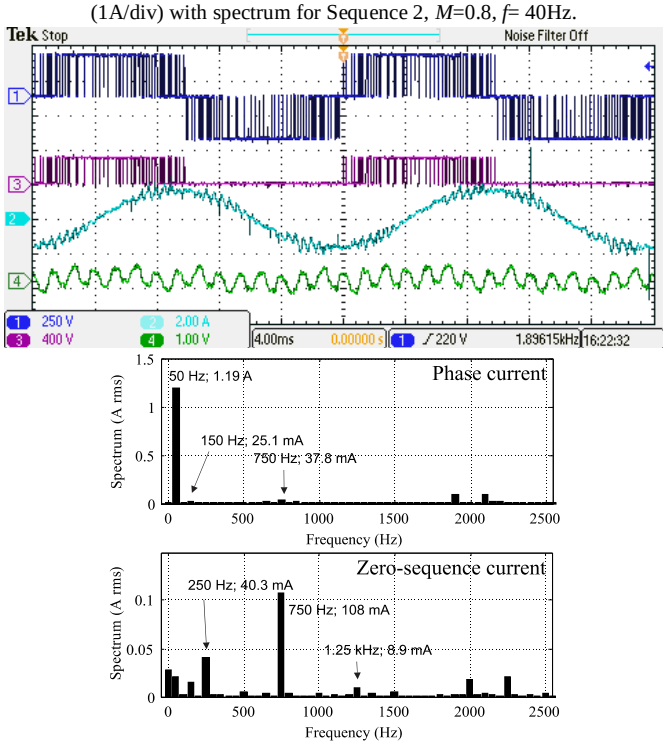

Fig. 12. Experimental results: phase voltage (250V/div), leg voltage (400V/div), phase current (2A/div) with spectrum, and zero-sequence current (1A/div) with spectrum for Sequence 2, M=1, f= 50Hz.

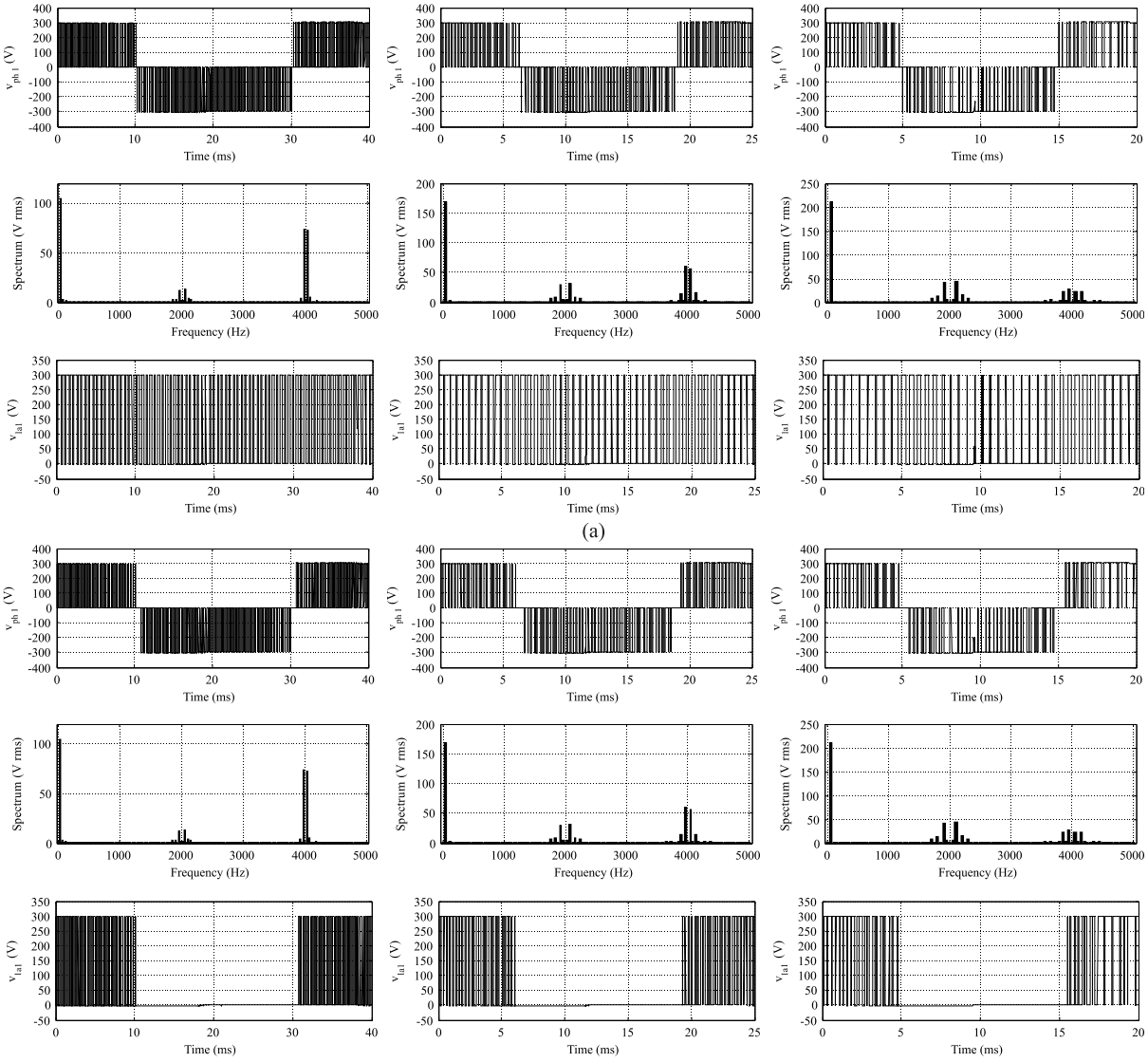

Fig. 13. Simulation results: phase voltage, its spectrum, and leg voltage for modulation indices M = 0.5, 0.8 and 1 (from left to right) for (a) Sequence 1 and (b) Sequence 2 (both with min-max injection).

frequency. The legs connected to the same phase are complementary in this manner; while one is clamped the other switches twice faster. An overall constant switching frequency is thus achieved in all leg pairs that form the individual H-bridges.

Comparison of the experimentally obtained phase voltage THDs is illustrated in Fig. 14. For benchmarking purposes, the THD obtained by using the same drive configuration, but with two isolated dc sources of 300 V each, in conjunction with phase disposition PWM (PD-PWM) from [5], is also shown. The THD was calculated according to:

$$THD = \sqrt{\sum_{i=2}^{r} V_i^2} \Big/ V_1^2 \qquad (7)$$

where r is adjusted to take into account harmonics up to the frequency of 21 kHz – the first ten switching frequency sidebands.

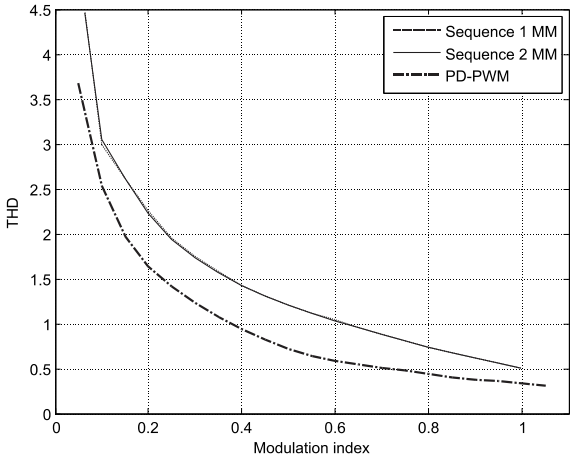

Fig. 14. Experimental results: THD of the phase voltage against modulation index.

Results for both sequences apply to the case with the injection of the min-max (MM) offset and fully overlap, as expected. The requirement to zero the CMV significantly reduces the number of space vectors and switching states that can be used, when compared to the equivalent configuration with two isolated dc sources. As a consequence, the THD performance is worse than the one reported in [5].

V. Zero-Sequence Current Analysis

The presence of the zero-sequence current is both undesirable and unexpected. On the basis of the theoretical considerations and having in mind that the CMV is eliminated by the applied switching states, it is expected that the zero-sequence current will also be zero. However, it has to be noted that the impedance in this topology for the zero-sequence component is very low, since it is composed of only stator resistance and stator leakage inductance. Hence any non-ideal property of the machine/inverter system can cause a significant current.

The harmonics in the zero-sequence current in Figs. 7-12 are of two types: i) harmonics that normally do not map into the-zero sequence axis, and, ii) zero-sequence harmonics. The first category includes the fundamental harmonic and the third harmonic (which is however of much lower values). The existence of non-zero fundamental in the zero-sequence current means that the five individual phase currents do not sum to zero. Since physics of the system do not impose such a constraint, this is not surprising. Each phase is in essence supplied from its own H-bridge inverter and there is no closed-loop control of any type. Hence any, no matter how minute, asymmetry between machine's phases and any difference in the semiconductor/inverter characteristics can lead to a slight imbalance of the fundamental current (and, similarly, the third harmonic which maps into the second plane). The highest value of the fundamental in the zero-sequence current is 68 mA in Fig. 7 (i.e. 13.6 mA per phase), which is small compared to the fundamental in the phase current of 1.19 A.

The second group of harmonics includes those that customarily map into the zero-sequence axis. On the basis of considerations in [14] and [15], three different causes for appearance of such harmonics can be identified: dead-time effect, voltage drops on semiconductors, and rotor slot harmonics.

The effect of the dead time and semiconductor voltage drop is explained using Fig. 15, Fig. 16, Table I and Table II. Fig. 15 shows one phase of the connected dc bus open-end topology. In each transfer between two switching states (zero to one or one to zero) of either inverter, on each side of the stator winding, the actual change of the voltage level can happen in the beginning or at the end of the dead-time interval. Since in these intervals both IGBTs associated with an inverter leg are turned off, the state taken by the inverter leg is determined by the diodes, or, in other words, the direction of the current flow. Considering the reference current direction indicated in Fig. 15, Table I summarizes the states taken during dead time by VSI*a* and VSI*b* with respect to the current direction.

The current flow direction also impacts on whether the voltage drop of the IGBT or the diode will be deducted or added to the desired output voltage (0 or V_{dc}). The considerations here can be decomposed in four different situations for each inverter, summarized in Table II. The first row of Table II assumes a positive current flow and high voltage state on both inverters. Since the current has to flow through the upper switch in the direction indicated in VSI*a* it will cause a voltage drop on the IGBT which has to be deducted from V_{dc}, while at VSI*b* side the current must flow through the upper diode and, according to its direction, causes a voltage drop that has to be added to V_{dc}.

Fig. 16 includes the observations above in the leg voltage waveforms of half of the switching period in the first and second sector for Sequence 1. Very much the same applies to Sequence 2. The plus and minus signs on the right-hand side in both sectors shown in Fig. 16 represent the current direction in accordance with $\pi/5$ lagging phase shift. The left columns denote the phase and inverter to which the shown waveform applies to, while the values $\pm V_{ce}$ and $\pm V_{df}$ indicate whether the IGBT collector-emitter or the diode forward voltage drop is to be added to or subtracted from the desired voltage at the output. The values obtained using (3) when these voltage drops are taken into consideration are $(V_{df}+V_{ce})/5$ in the first sector and all other odd sectors, and $-(V_{df}+V_{ce})/5$ in the second and all other even sectors. These considerations are graphically shown as CM1 waveform in Fig. 16. CM2 in Fig. 16 is the waveform that is the consequence of the difference in the instant of the leg voltage change during dead time. Both of these effects cause a CMV that alternates from sector to sector, causing a voltage alternating five times faster than the fundamental. Since the common-mode voltage, which normally appears between the two negative rails of the two inverters, is short-circuited in the connected dc bus topology, the effect leads to the zero-

TABLE I: Inverter output voltage during dead time.

Inverter *a*: current direction	Dead-time state
+	0
-	1

Inverter *b*: current direction	Dead-time state
+	1
-	0

TABLE II: Alteration of inverter output voltage caused by semiconductor voltage drop.

Inverter *a* state and current direction	V_{1N} (=v_{la})
1, +	V_{dc}-V_{ce}
1, -	V_{dc}+V_{df}
0, +	0-V_{df}
0, -	0+V_{ce}

Inverter *b* state and current direction	V_{2N} (=v_{lb})
1, +	V_{dc}+V_{df}
1, -	V_{dc}-V_{ce}
0, +	0+V_{ce}
0, -	0-V_{df}

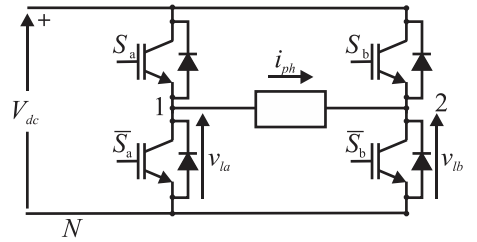

Fig. 15. Schematic of one phase of the connected dc bus open-end topology.

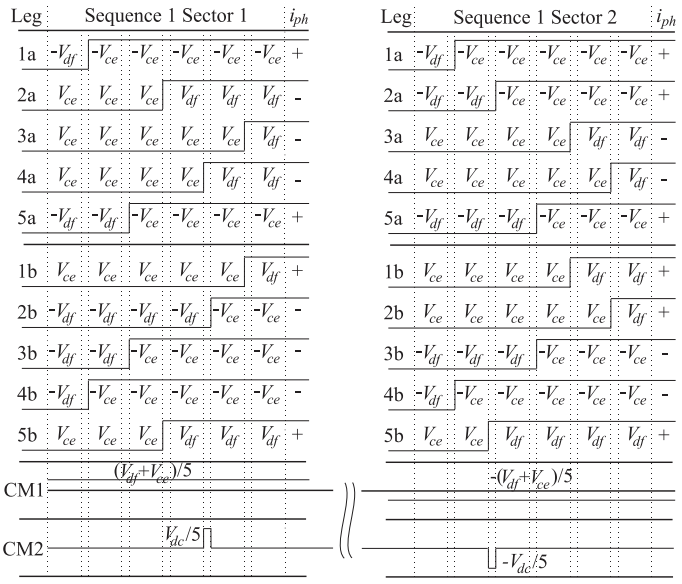

Fig. 16. Graphical analysis of semiconductor voltage drop and dead-time effect.

sequence current. The net result is the fifth harmonic in the zero-sequence current.

Another significant component appears in the zero-sequence current, around the fifteenth harmonic. While the fifth harmonic was also present in the simulation study, the component around the 15th harmonics was non-existent in the simulations. This harmonic is believed to be caused by the rotor slot harmonics of the machine. The slot harmonics appear at frequencies [14]:

$$\omega_{sh} = (Z / P)\omega_r \pm \omega_0 \tag{8}$$

where ω_{sh} is the harmonic angular frequency, ω_r the rotor speed, ω_0 the synchronous speed, p = 2 the number of pole pairs and Z = 28 the number of rotor slots. Since the rotor runs under no-load conditions, rotor speed is practically equal to the synchronous speed. It follows from (8) that the dominant stator current slot harmonic is positioned near to the 15th multiple of the synchronous speed. The existence of this harmonic is the particular feature of the machine used here and this does not represent a general situation.

In order to compare the modulation methods obtained by the application of the two sequences, Figs. 17 and 18 depict the amounts of the fifth and the fifteenth harmonic of the zero-sequence current, respectively. In Fig. 19 the RMS of the fundamental of the phase current is displayed to give a measure of comparison to Figs. 17-18.

The fifth harmonic of the zero-sequence current reaches significant values at low modulation indices, where, due to the *V/f* control, a larger number of switchings in a particular sector helps to build up a larger stator current harmonic. This is especially noticeable for Sequence 1. At large modulation indices the fifth harmonic reduces to more acceptable values.

The fifteenth harmonic increases with modulation index (i.e. stator fundamental frequency). At first, at low modulation indices, it is lower than the fifth harmonic, but it becomes dominant at high modulation index values.

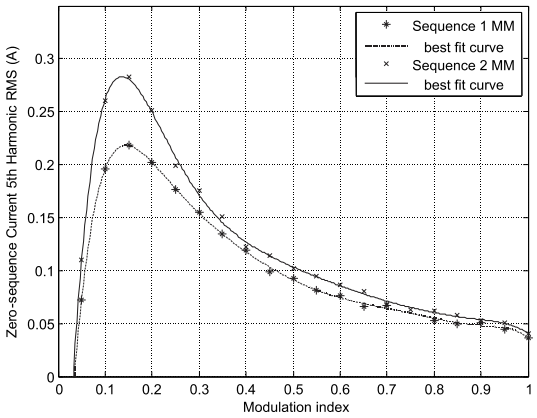

Fig. 17. Experimental results: zero-sequence current 5th harmonic RMS against modulation index.

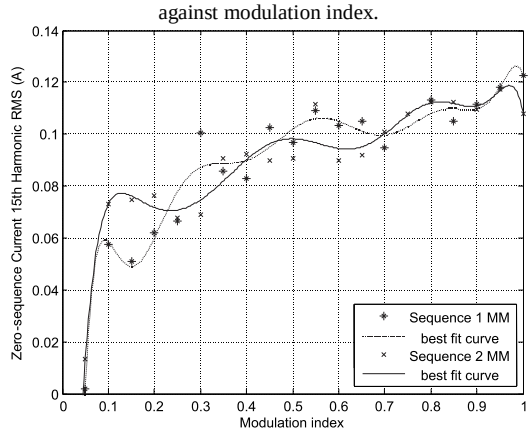

Fig. 18. Experimental results: zero-sequence current 15th harmonic RMS against modulation index.

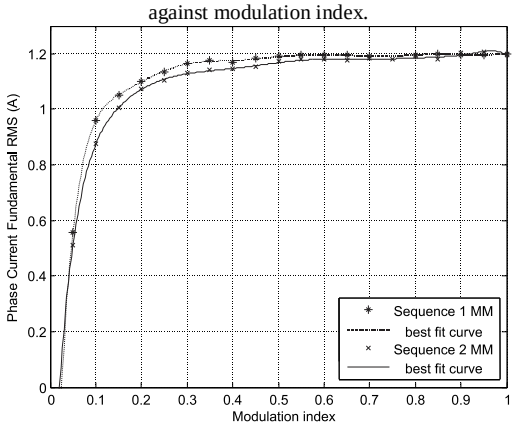

Fig. 19. Experimental results: phase current fundamental RMS against modulation index.

The last conducted experimental test serves the purpose of verifying the theoretical considerations related to Fig. 16 and the dead-time effect. Sequence 1 is used again. However, instead of the common dc-source topology, the structure with two isolated dc voltage sources (300 V each) is used and the CMV is measured between the negative rails of the configuration. To eliminate the impact of non-ideal machine characteristics, pure *R* load is used. Fig. 20 shows the phase voltage and the CMV, which should be zero, for operation at 0.8 modulation index (40 Hz). As can be seen, the CMV has only very short spikes, commensurate with the dead-time interval, and the value of the spikes is 60 V, as predicted in

the last row of Fig. 16 (V_{dc}/5 = 60 V). The frequency is clearly the one of the fifth harmonic and the average value is zero.

Since the drive system discussed in the paper is most likely to be used in practice in vector controlled mode, the best method for zero-sequence current elimination appears to be use of closed-loop current control. It has been demonstrated in [15] that use of two pairs of current controllers enables excellent compensation of both asymmetries and the dead-time effect in the five-phase drive with isolated neutral point and single-sided supply. Since here one has five rather than four (as in [15]) degrees of freedom, this means that the current control of the drive would have to involve five rather than four current controllers.

VI. Conclusion

The paper has presented two modulation methods for the five-phase open-end topology with CMV elimination. The approach is based on the principles used for three-phase topologies. It is shown that many possibilities exist regarding switching state selection in the five-phase structure. Theoretical considerations are verified by means of experimental results. Although the modulation methods are aimed at full CMV elimination and should therefore ensure absence of any zero-sequence current, parasitic effects due to the non-ideal nature of the inverter and the motor cause the flow of zero-sequence current. These effects have also been addressed in detail.

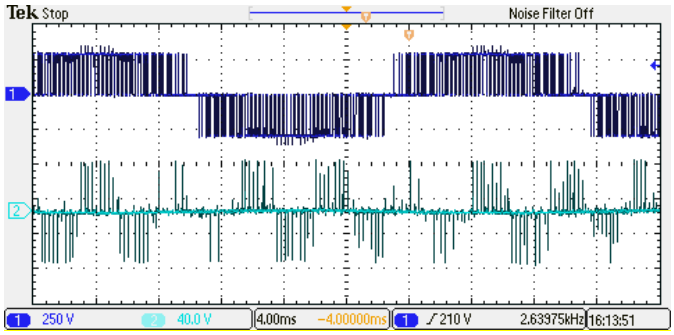

Fig. 20. Sequence 1 applied to the isolated dc-bus topology: phase voltage and CM voltage at 0.8 modulation index (40 Hz) with 300 V dc sources.

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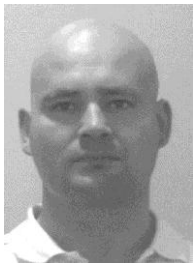

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