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**Partida-Manzanera, T, Zaidi, ZH, Roberts, JW, Dolmanan, SB, Lee, KB, Houston, PA, Chalker, PR, Tripathy, S and Potter, RJ**

**Comparison of atomic layer deposited Al<sub>2</sub>O<sub>3</sub> and (Ta<sub>2</sub>O<sub>5</sub>)<sub>0.12</sub>(Al<sub>2</sub>O<sub>3</sub>)<sub>0.88</sub> gate dielectrics on the characteristics of GaN-capped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors**

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# Comparison of atomic layer deposited $\text{Al}_2\text{O}_3$ and $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$ gate dielectrics on the characteristics of GaN-capped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors

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# Comparison of atomic layer deposited $\text{Al}_2\text{O}_3$ and $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$ gate dielectrics on the characteristics of GaN-capped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors

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## ABSTRACT

The current research investigates the potential advantages of replacing  $\text{Al}_2\text{O}_3$  with  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  as a higher dielectric constant ( $\kappa$ ) gate dielectric for GaN-based metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs). The electrical characteristics of GaN-capped AlGaN/GaN MOS-HEMT devices with  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  as the gate dielectric are compared to devices with  $\text{Al}_2\text{O}_3$  gate dielectric and devices without any gate dielectric (Schottky HEMTs). Compared to the  $\text{Al}_2\text{O}_3$  MOS-HEMT, the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT achieves a larger capacitance and a smaller absolute threshold voltage, together with a higher two-dimensional electron gas carrier concentration. This results in a superior improvement of the output characteristics with respect to the Schottky HEMT, with higher maximum and saturation drain current values observed from DC current-voltage measurements. Gate transfer measurements also show a higher transconductance for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT. Furthermore, from OFF-state measurements, the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT shows a larger reduction of the gate leakage current in comparison to the  $\text{Al}_2\text{O}_3$  MOS-HEMT. These results demonstrate that the increase in  $\kappa$  of  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  compared with  $\text{Al}_2\text{O}_3$  leads to enhanced device performance when the ternary phase is used as a gate dielectric in the GaN-based MOS-HEMT.

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## I. INTRODUCTION

Wide bandgap semiconductors such as GaN have a high breakdown field strength, making them very attractive for high-frequency, high-power, and high-temperature power electronic applications.<sup>1,2</sup> Most commercial GaN-based devices available today are based on high electron mobility transistor (HEMT) structures.<sup>3</sup> These devices provide a highly conductive two-dimensional electron gas (2DEG) formed at the heterojunction between GaN and a wider bandgap

material such as AlGaN as a result of spontaneous and piezoelectric polarization effects.<sup>4</sup> AlGaN/GaN HEMTs have attracted much attention in the past few years for power switching applications in the medium voltage market (600–1200 V) and radio frequency (RF) applications due to their higher conversion efficiency and higher switching frequency when compared to conventional Si power devices.<sup>5–7</sup> One of the major issues remaining for AlGaN/GaN HEMTs is the high leakage current through the Schottky gate which

causes device performance and reliability issues, as well as increase device losses in the OFF-state.<sup>8–10</sup> To reduce the gate leakage current, wide bandgap, high dielectric constant (high- $\kappa$ ) oxides such as  $\text{Al}_2\text{O}_3$ ,<sup>11–14</sup>  $\text{HfO}_2$ ,<sup>15–17</sup>  $\text{ZrO}_2$ ,<sup>17,18</sup> and  $\text{Ta}_2\text{O}_5$ <sup>19</sup> have been used to produce metal-oxide-semiconductor HEMTs (MOS-HEMTs) structures.  $\text{Al}_2\text{O}_3$  is currently one of the most widely exploited gate dielectrics for GaN-based MOS-HEMTs due to its large bandgap (6.5 eV),<sup>20</sup> large breakdown electric field (5–10 MV/cm),<sup>21</sup> and good chemical and thermal stability. The main limitation of  $\text{Al}_2\text{O}_3$  as a gate oxide is its modest permittivity ( $\kappa \sim 9$ ).<sup>22</sup> Traditional high- $\kappa$  dielectrics such as  $\text{HfO}_2$  ( $\kappa \sim 18$ )<sup>22</sup> and  $\text{ZrO}_2$  ( $\kappa \sim 20$ )<sup>23</sup> have a significantly higher permittivity than  $\text{Al}_2\text{O}_3$ , but this comes at the expense of a smaller bandgap,<sup>23,24</sup> which can increase carrier leakage if the barrier height between the insulator and the semiconductor is too low. Compared to  $\text{HfO}_2$  and  $\text{ZrO}_2$ ,  $\text{Ta}_2\text{O}_5$  has shown some promise as a high- $\kappa$  ( $\kappa \sim 25$ )<sup>25</sup> gate dielectric for GaN-based devices, with high breakdown electric field (4.5 MV/cm) and relatively low gate leakage despite its lower bandgap (4.4 eV).<sup>18,19,26</sup> Our previous research has shown that the combination of wide bandgap  $\text{Al}_2\text{O}_3$  with a higher  $\kappa$  material such as  $\text{Ta}_2\text{O}_5$  can achieve a higher  $\kappa$  value with respect to  $\text{Al}_2\text{O}_3$  together with a sufficient conduction band offset (CBO) to the GaN-HEMT (>1 eV) for electron confinement,<sup>27</sup> which could allow a further reduction of the gate leakage while maintaining or enhancing the device gate capacitance. In this paper, the optimum composition selected for the ternary oxide was  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$ . This is based on preliminary band alignment studies where the band offsets between  $(\text{Ta}_2\text{O}_5)_x(\text{Al}_2\text{O}_3)_{1-x}$  ( $0 \leq x \leq 1$ ) films and GaN-on-Si substrate were analyzed as a function of the  $x$  molar fraction (shown in the [supplementary material](#)). The aim of the selection process was to maximize the  $\kappa$  value of the oxide by maximizing the  $\text{Ta}_2\text{O}_5$  molar fraction while also ensuring that the band offsets between the oxide and GaN did not fall below 1 eV. To evaluate how the introduction of this ternary gate oxide affects the performance of GaN-based HEMT devices, this paper presents a comparative study of the electrical characteristics of GaN-capped AlGaIn/GaN HEMTs with the standard Schottky gate and MOS-HEMTs with either  $\text{Al}_2\text{O}_3$  or  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  gate dielectrics.

## II. EXPERIMENTAL DETAILS

[Figure 1](#) shows the schematics of the AlGaIn/GaN Schottky gate HEMT and the MOS-HEMT devices used in the present study. The  $\text{Al}_x\text{Ga}_{1-x}\text{N}$ /GaN HEMT stack was grown on a 150 mm diameter (1.0 mm thick) Si(111) substrate using an Aixtron close-coupled showerhead metal organic chemical vapor deposition system. The total thickness of the nitride HEMT stack is about 3.6  $\mu\text{m}$ . It consists of an  $\sim 280$  nm thick high-temperature AlN layer, followed by three step-graded  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  intermediate layers with Al composition tuned from 58% to 20%, followed by an uninterrupted growth of a GaN buffer with a thickness of about 1.3  $\mu\text{m}$  and an undoped GaN channel layer of 500 nm in thickness. The GaN buffer grown is unintentionally C-doped. The top HEMT layers comprise a thin AlN spacer layer  $\sim 1.0$  nm thick, an  $\sim 20$  nm thick  $\text{Al}_{0.23}\text{Ga}_{0.77}\text{N}$  barrier layer, and a thin  $\sim 2$  nm GaN cap layer.

The average full width at half maximum (FWHM) of the GaN (002) and (102) rocking curves obtained from high-resolution X-ray

diffraction measurements were 518 and 1540 arc sec, respectively, indicative of device grade GaN layers on 150 mm Si(111).<sup>28</sup> Atomic force microscopy showed very smooth surface morphology, with an arithmetic average root mean square roughness of 0.15 nm measured in a  $5 \times 5 \mu\text{m}^2$  scan area. From Hall-effect measurements at room temperature, the sheet density of the resultant 2DEG was in the order of  $\sim 6.5\text{--}7.7 \times 10^{12} \text{ cm}^{-2}$  and the electron mobility was about  $\sim 1300\text{--}1400 \text{ cm}^2/\text{V s}$ .

To fabricate the devices, mesa isolation was performed using inductively coupled plasma (ICP) etching with a  $\text{Cl}_2$ -based plasma to etch around 350 nm. A Ti/Al/Ni/Au metal stack was thermally evaporated onto the sample and annealed at 830  $^\circ\text{C}$  under  $\text{N}_2$  ambient to form the source and drain ohmic contacts. The contact resistance extracted from transmission line model measurements<sup>29</sup> was in the range of 0.5–0.9  $\Omega \text{ mm}$ . A  $\text{SiN}_x$  passivation layer of  $\sim 80$  nm was deposited using plasma-enhanced chemical vapor deposition, and 1.5  $\mu\text{m}$  gate windows were opened by etching through the  $\text{SiN}_x$  layer using ICP etching. For the MOS-HEMT devices,  $\sim 10$  nm thick  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  gate oxides were deposited at 250  $^\circ\text{C}$  by atomic layer deposition (ALD) using an Oxford OpAL thermal ALD reactor. Trimethylaluminum (TMA), pentakis(dimethylamino)tantalum (PDMAT), and de-ionized water ( $\text{H}_2\text{O}$ ) were used as the aluminum, tantalum, and oxygen sources, respectively. Tantalum doping was achieved using delta doping where every three cycles of TMA and  $\text{H}_2\text{O}$  (20 ms TMA dose/5 s purge/20 ms  $\text{H}_2\text{O}$  dose/5 s purge) were followed by a cycle of PDMAT and  $\text{H}_2\text{O}$  (4 s PDMAT dose/5 s purge/20 ms  $\text{H}_2\text{O}$  dose/5 s purge). The measured growth rates for the  $\text{Al}_2\text{O}_3$  and  $\text{Ta}_2\text{O}_5$  ALD processes were about 0.9  $\text{\AA}/\text{cycle}$  and 0.76  $\text{\AA}/\text{cycle}$ , respectively. The gate oxides were grown using a total of 120 ALD cycles. The samples were then annealed at 600  $^\circ\text{C}$  for 60 s under  $\text{N}_2$  ambient to improve the interface between the gate dielectric and the semiconductor surface (see Ref. 27 for more details). Following this, T-shape Ni/Au gate metal electrodes with 100  $\mu\text{m}$  gate width were deposited by thermal evaporation. The final devices have a gate-source separation of 2.5  $\mu\text{m}$ , a gate-drain separation of 12  $\mu\text{m}$ , and a gate field plate extension of 1  $\mu\text{m}$  toward both the drain and the source. For the present study, a minimum number of five devices were measured for each structure. The data presented are representative of the typical behaviors observed for each of the three structures.

## III. RESULTS AND DISCUSSION

### A. Input characteristics

The gate-source capacitance for the Schottky HEMT ( $C_{\text{GS}}^{\text{HEMT}}$ ) can be modeled as a series capacitance of the AlN spacer ( $C_{\text{AIN}}$ ), the AlGaIn barrier ( $C_{\text{AlGaIn}}$ ), and the GaN cap ( $C_{\text{GaN}}$ ) [[Fig. 1\(a\)](#)]. For the MOS-HEMTs, it is assumed that the gate oxide contributes an additional series capacitance to the gate structure [[Fig. 1\(b\)](#)]. The MOS-HEMTs gate-source capacitance ( $C_{\text{GS}}^{\text{MOS-HEMT}}$ ) can, therefore, be described by

$$1/C_{\text{GS}}^{\text{MOS-HEMT}} = 1/C_{\text{AIN}} + 1/C_{\text{AlGaIn}} + 1/C_{\text{GaN}} + 1/C_{\text{ox}}, \quad (1)$$

where  $C_{\text{AIN}} = \kappa_{\text{AIN}} \cdot \epsilon_0 \cdot A/t_{\text{AIN}}$ ,  $C_{\text{AlGaIn}} = \kappa_{\text{AlGaIn}} \cdot \epsilon_0 \cdot A/t_{\text{AlGaIn}}$ ,  $C_{\text{GaN}} = \kappa_{\text{GaN}} \cdot \epsilon_0 \cdot A/t_{\text{GaN}}$ , and  $C_{\text{ox}} = \kappa_{\text{ox}} \cdot \epsilon_0 \cdot A/t_{\text{ox}}$ .  $\kappa$  and  $t$  are

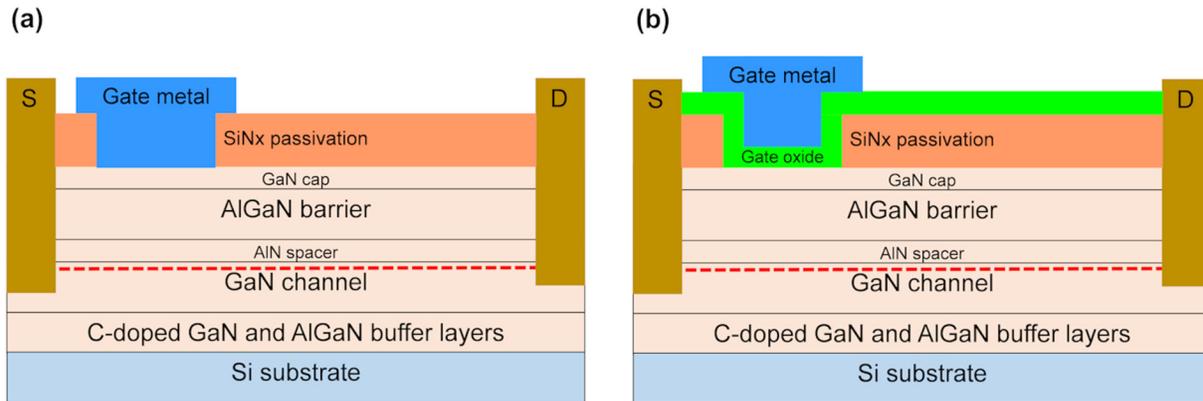


FIG. 1. Schematic of the cross section of the (a) Schottky gate AlGaIn/GaN HEMT and (b) AlGaIn/GaN MOS-HEMT structures used in the present study.

the relative permittivity and thickness of the layers,  $\epsilon_0$  is the permittivity of free space, and  $A$  is the area of the gate.

Figure 2 shows the gate-source capacitance ( $C_{GS}$ ) of  $\sim 100 \times 160 \mu\text{m}^2$  area Schottky and MOS-HEMTs obtained as a function of the gate-source voltage ( $V_{GS}$ ), using C-V measurements at 10 kHz with  $V_{GS}$  swept from  $-6$  V to  $+1$  V. As expected, the accumulation capacitance for the MOS-HEMT devices is significantly less than that of the Schottky HEMT (Fig. 2), which is in agreement with Eq. (1). It can be observed that the capacitance of the Schottky HEMT dramatically increases above 0.5 V. This is attributed to charge overflow from the 2DEG channel,<sup>30</sup> which decreases the effective barrier layer thickness. The accumulation  $C_{GS}$  values obtained for the three devices range from

$4.3 \times 10^{-3}$  F/m<sup>2</sup> for the Schottky HEMT to  $2.6 \times 10^{-3}$  F/m<sup>2</sup> for the  $\text{Al}_2\text{O}_3$  MOS-HEMT and  $2.8 \times 10^{-3}$  F/m<sup>2</sup> for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT. Using the measured  $C_{GS}$  values and Eq. (1), the  $\kappa$  values calculated for the  $\sim 10$  nm thick  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  layers are 7.2 and 9.8, respectively. The increase in the permittivity of the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  with respect to that of the  $\text{Al}_2\text{O}_3$  is in agreement with our previous study where the permittivity of the  $(\text{Ta}_2\text{O}_5)_x(\text{Al}_2\text{O}_3)_{1-x}$  layers on Si was measured as a function of the  $\text{Ta}_2\text{O}_5$  molar fraction.<sup>27</sup>

The reduction in  $C_{GS}$  following the introduction of the gate oxide is equivalent to a reduced ability to deplete the 2DEG channel with a given bias. A higher  $V_{GS}$  is, therefore, needed to “pinch-off” the channel in the MOS-HEMTs compared to the Schottky HEMT. This is reflected by a significant increase in the absolute threshold voltage ( $V_{th}$ ) value<sup>31</sup> extracted from the C-V characteristics (Fig. 2). Assuming the same sheet charge density in the channel for the Schottky HEMT and the MOS-HEMTs at zero gate bias and not taking into account the surface charge at the oxide/GaN interface, the  $V_{th}$  absolute value of the MOS-HEMTs ( $V_{th}^{MOS-HEMT}$ ) increases with respect to that of the HEMT ( $V_{th}^{HEMT}$ ) as follows:<sup>31</sup>

$$Q_S = q N_S = C_{GS}^{MOS-HEMT} \times V_{th}^{MOS-HEMT} = C_{GS}^{HEMT} \times V_{th}^{HEMT}, \quad (2)$$

$$V_{th}^{MOS-HEMT} = V_{th}^{HEMT} (C_{GS}^{HEMT} / C_{GS}^{MOS-HEMT}), \quad (3)$$

where  $Q_S$  is the charge at the metal/oxide and metal/semiconductor interfaces and  $N_S$  is the 2DEG sheet carrier density.

A negative shift in the  $V_{th}$  can be observed for the MOS-HEMT devices (Fig. 2), which is in agreement with Eq. (3). The  $V_{th}$  decreases from  $-1.4$  V for the Schottky HEMT to  $-3.5$  V and  $-3.3$  V for the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs, respectively. The theoretical  $V_{th}$  values from Eq. (3) for the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs are  $-2.3$  V and  $-2.1$  V, respectively, which are 1.2 eV smaller than the values obtained

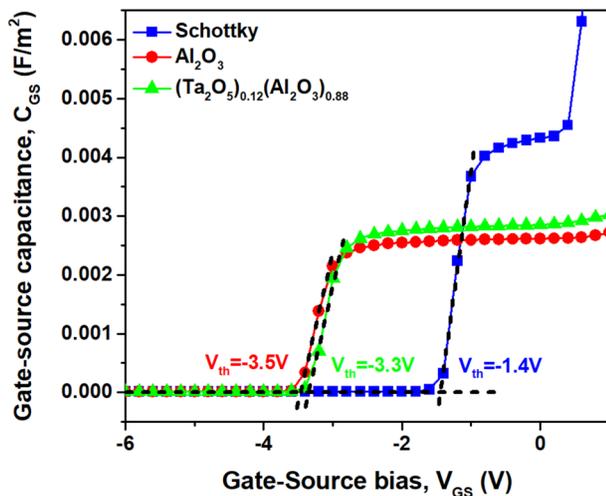


FIG. 2. C-V measurements at 10 kHz for  $\sim 100 \times 160 \mu\text{m}^2$  area Schottky gate HEMT and MOS-HEMT structures fabricated with  $\sim 10$  nm thick  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  gate oxides.

experimentally. The difference between the experimental and calculated values is attributed to fixed oxide charges due to oxide/GaN interface states and/or bulk oxide traps.<sup>30–32</sup> The  $V_{th}$  shift caused by the interface charge is the same for both the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs. This is attributed to the fact that initial ALD cycles for the growth of  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  were  $\text{Al}_2\text{O}_3$  cycles; hence, the tantalum dopant ions are not directly in contact with the semiconductor. The results show that the smaller  $V_{th}$  absolute value obtained for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT in comparison to the  $\text{Al}_2\text{O}_3$  MOS-HEMT is related to the bigger  $C_{GS}$  achieved using a higher  $\kappa$  gate dielectric.

The 2DEG sheet carrier concentration ( $n_s$ ) of the HEMTs for a given gate bias and low electric fields can be approximated by a simple analytical model by Thayne *et al.*,<sup>33</sup>

$$n_s = [C_{GS}/q] \times [V_{GS} - V_{th}]. \quad (4)$$

Figure 3 shows  $n_s$  of the three devices as a function of  $V_{GS}$ , obtained from the C-V measurements. The results show that  $n_s$  is a linear function of  $V_{GS}$  for voltages beyond the  $V_{th}$  (Fig. 3), which is in accordance with Eq. (4). The exception to this is for the Schottky HEMT at  $V_{GS}$  values above 0.5 V, where the slope increases due to the charge overflow from the 2DEG channel<sup>30</sup> discussed earlier. It can be observed that  $n_s$  of the MOS-HEMTs is higher than  $n_s$  of the Schottky HEMT for voltages  $V_{th} < V < 0.5$  V. This experimental increase observed for the  $n_s$  in the active region of the MOS-HEMTs is explained by the fact that the reduction of  $C_{GS}$  does not exactly correspond to the increase of the  $V_{th}$  [Eq. (4)]. The increase in  $n_s$  is believed to be caused by either the gate oxide's passivation effect in the gate region, which reduces the number of GaN surface states that can trap electrons leading to less electron depletion in the 2DEG,<sup>34,35</sup> or by the increase in positive charge/reduction in negative charge at the oxide/GaN interface after oxide deposition, which neutralizes

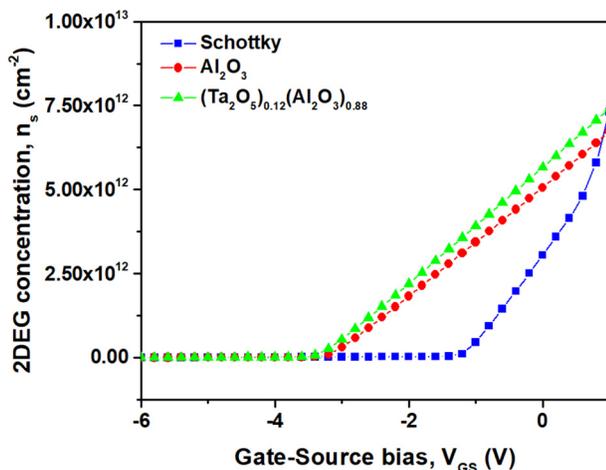


FIG. 3.  $n_s$  as a function of the  $V_{GS}$  obtained from C-V measurements at 10 kHz for the  $\sim 100 \times 160 \mu\text{m}^2$  area Schottky gate HEMT and MOS-HEMT structures fabricated with  $\sim 10$  nm thick  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  gate oxides.

the fixed polarization charge.<sup>34</sup> The results indicate that  $n_s$  depends on the gate dielectric properties. For a given  $V_{GS}$ ,  $n_s$  of the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT is bigger than  $n_s$  of the  $\text{Al}_2\text{O}_3$  MOS-HEMT. In fact, from Eq. (4), the slope of the  $n_s$  can be approximated as<sup>32</sup>

$$\frac{\partial n_s}{\partial V_{GS}} = C_{GS}/q. \quad (5)$$

Thus, the decrease in the  $n_s$  slope observed for the MOS-HEMTs is due to smaller  $C_{GS}$  obtained after the introduction of the gate dielectrics, which is in agreement with the simple HEMT analytical model.

## B. ON-state output characteristics

### 1. Direct-current current-voltage characteristics

The drain current ( $I_D$ ) of a HEMT can be described as<sup>36</sup>

$$I_D = q \times W_G \times n_s \times v, \quad (6)$$

where  $W_G$  is the gate width and  $v$  is the 2DEG charge carrier velocity.

Figure 4 shows a comparison of the current-voltage (I-V) characteristics under DC biasing for the three devices, for various  $V_{GS}$  values between  $-4$  V and  $+2$  V, in steps of 2 V. The pinch-off voltage is  $-2$  V for the Schottky HEMT and  $-4$  V for the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs. In several of the data sets,  $I_D$  reaches a maximum and then decreases slightly with a further increase in  $V_{DS}$ . This is attributed to self-heating arising from the poor thermal conductivity of the Si substrate.<sup>37</sup>

An increase in the MOS-HEMTs maximum  $I_D$  at a positive gate bias is observed (Fig. 4), which is consistent with Eq. (6). When a  $V_{GS} = +2$  V is applied, the maximum drain saturation

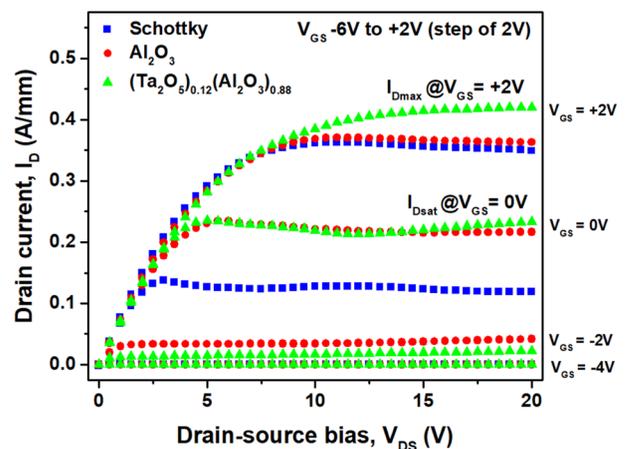


FIG. 4. Output I-V characteristics of the Schottky HEMT and the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs showing  $I_D$  as a function of  $V_{DS}$  for varying  $V_{GS}$  between  $-6$  V and  $+2$  V in steps of  $+2$  V.



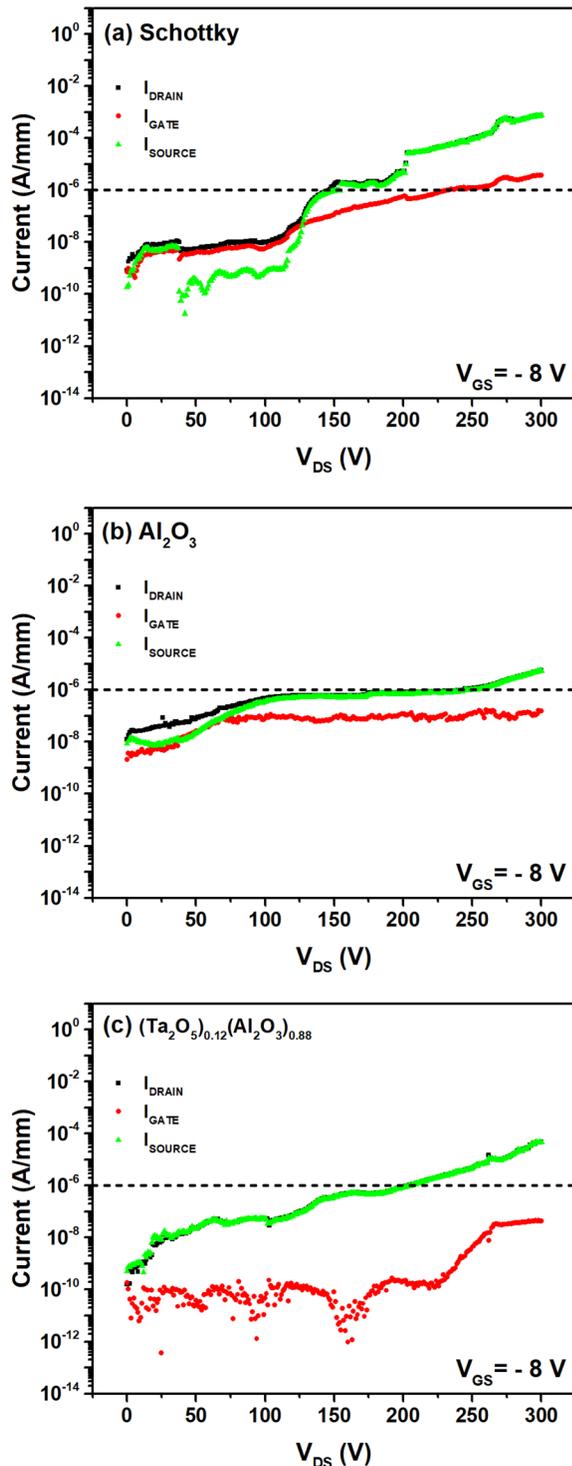


FIG. 6. Three-terminal OFF-state measurements of the (a) Schottky HEMT, (b)  $\text{Al}_2\text{O}_3$  MOS-HEMT, and (c)  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT with  $V_{GS} = -8$  V and  $V_{DS}$  swept from  $-0$  V to  $+300$  V.

2DEG channel. Therefore, the bigger  $g_m$  obtained for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT in comparison to the  $\text{Al}_2\text{O}_3$  MOS-HEMT is an indicator of superior channel control.

The devices output  $I_D$  and gate current ( $I_G$ ) are shown in Fig. 5(b), as a function of  $V_{GS}$  at  $V_{DS} = +10$  V. The  $I_D$  ON-OFF ratio of the three devices is limited by the OFF-state drain leakage current likely dominated by horizontal source-drain leakage via buffer<sup>42</sup> rather than  $I_G$ . When  $V_{GS}$  is  $-6$  V,  $I_D$  of the Schottky HEMT is below  $4 \times 10^{-7}$  A/mm, whereas  $I_D$  of the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs is below  $2 \times 10^{-6}$  A/mm. This results in an  $I_D$  ON-OFF ratio of around  $10^6$  for the Schottky HEMT and  $10^5$  for the MOS-HEMTs. On the other hand,  $I_G$  of the three devices remains reasonably stable below  $\sim 10^{-9}$  A/mm for  $V_{GS}$  values up to  $+1$  V. The MOS-HEMTs and the Schottky HEMT show similar  $I_G$  values due to the measurements minimum current limit at a low voltage regime ( $< +10$  V). However, for  $V_{GS}$  values above  $+1$  V,  $I_G$  of the Schottky HEMT starts to increase rapidly. This indicates that the substitution of the gate Schottky barrier by a MOS structure can effectively reduce the ON-state gate leakage.<sup>34</sup>

### C. OFF-state output characteristics

Figure 6 shows the three-terminal OFF-state I-V characteristics of the three devices, obtained by sweeping  $V_{DS}$  from  $0$  V to  $300$  V with  $V_{GS}$  kept at  $-8$  V. The substrates were not grounded during the measurements. From Fig. 6(a), it can be observed that the gate leakage current ( $I_{GATE}$ ) of the Schottky gate HEMT structure dominates when  $V_{DS}$  is below  $130$  V, and the leakage between the source and the drain terminals ( $I_{SOURCE}$ ) overtakes  $I_{GATE}$  for voltages above  $130$  V.  $I_{GATE}$  surpasses  $1 \mu\text{A}/\text{mm}$  for voltages above  $233$  V. For the MOS-HEMTs [Figs. 6(b) and 6(c)],  $I_{GATE}$  is smaller than  $I_{SOURCE}$  up to  $300$  V. This means that  $I_{GATE}$  is not the main source of leakage in the MOS-HEMTs for the range of  $V_{DS}$  measured. In addition to this,  $I_{GATE}$  remains below  $1 \mu\text{A}/\text{mm}$  up to  $300$  V. Compared to the Schottky HEMT,  $I_{GATE}$  of the MOS-HEMTs is significantly less at  $V_{DS} = 300$  V. For the Schottky gate device,  $I_{GATE}$  at  $V_{DS} = 300$  V is found to be below  $4 \times 10^{-6}$  A/mm, whereas  $I_{GATE}$  of the  $\text{Al}_2\text{O}_3$  and  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMTs are under  $1.5 \times 10^{-7}$  A/mm and  $4.3 \times 10^{-8}$  A/mm at  $V_{DS} = 300$  V, respectively. Thus, a reduction of the OFF-state gate leakage current is achieved by introducing the gate oxides, with an observed decrease of over one order of magnitude for the  $\text{Al}_2\text{O}_3$  MOS-HEMT and a higher decrease of over two orders of magnitude for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT.

### IV. CONCLUSIONS

The electrical characteristics of a GaN-capped AlGaN/GaN Schottky HEMT and MOS-HEMTs with either  $\text{Al}_2\text{O}_3$  or  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  gate oxides have been analyzed. The MOS-HEMTs show a smaller gate capacitance and bigger absolute threshold voltages than an equivalent Schottky HEMT device due to the larger gate-to-channel separation and the charge induced at the oxide/GaN interface. However, compared to the  $\text{Al}_2\text{O}_3$  MOS-HEMT, the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT achieves a bigger capacitance and a smaller absolute threshold voltage, improving the gate modulation efficiency and reducing power consumption during switching. This in turn results in a higher 2DEG

concentration for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT compared with those of the Schottky HEMT and the  $\text{Al}_2\text{O}_3$  MOS-HEMT, increasing its saturation drain current, which gives superior device power output. The maximum transconductance of the  $\text{Al}_2\text{O}_3$  MOS-HEMT compared to the Schottky HEMT decreases, whereas the maximum transconductance of the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT remains similar, which indicates better channel control. The MOS-HEMTs also show a significant reduction of the gate leakage current [over one order of magnitude for the  $\text{Al}_2\text{O}_3$  MOS-HEMT and over two orders of magnitude for the  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  MOS-HEMT, when the drain-source voltage is 300 V]. Hence, as well as larger gate leakage current suppression, the use of  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  increases  $\kappa$  of the gate dielectric, further improving the MOS-HEMT electrical performance.

### SUPPLEMENTARY MATERIAL

See the [supplementary material](#) for the band offsets between  $(\text{Ta}_2\text{O}_5)_{0.12}(\text{Al}_2\text{O}_3)_{0.88}$  ( $0 \leq x \leq 1$ ) films and GaN-on-Si substrate as a function of the  $x$  molar fraction.

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