Challenge and solution for characterizing NBTI-generated defects in nanoscale devices

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***Abstract*- Negative bias temperature instability (NBTI) is a well known ageing process for CMOS technologies. Many early works were focused on large devices where device-to-device variations (DDV) are negligible. As device sizes downscale to nanometers, DDV becomes substantial. NBTI is a stochastic process and causes a time-dependent DDV. Characterizing the NBTI-generated defects in nanoscale devices has two main challenges. First, current fluctuates with time and this introduces uncertainties in measurements. Second, the test time is long and costly: to characterize the NBTI-induced DDV, it is essential to repeat the same test on multiple devices. This work reviews recent progresses in addressing these issues. Based on the As-grown-Generation (AG) model, it will be shown that the measurement uncertainties are dominated by As-grown hole traps and can be removed by subtracting the average value. To reduce the test time, the voltage step stress (VSS) technique is combined with the Stress-Discharge -Recharge (SDR) method. This VSS-SDR technique reduces test time to within one hour per device. The model extracted by VSS-SDR is verified by comparing its prediction with the test data obtained under conventional constant voltage stress.**

***Keywords** – Negative bias temperature instability, NBTI, Device variations, Time-dependent variations, Traps, Positive charges, Ageing, Degradation, Device lifetime, Nanoscale devices.*

I. Introduction

Negative bias temperature instability (NBTI) originates from both generated interface states and positive charges formed in the gate dielectric [1-8]. It mainly degrades the performance of pMOSFETs, causing an increase of threshold voltage and a reduction of driving current. Many early research [2-8] focused on large devices, where the device-to-device variation (DDV) and current fluctuation shown in Fig. 1a is negligible. Modern CMOS technologies, however, use nanoscale devices. The challenges for characterizing the NBTI of nanoscale devices include uncertainties in measurements and long test time.

In a typical NBTI test, the stress is interrupted at pre-set time to monitor the degradation from an Id-Vg measurement. For large device, Id before the interruption does not fluctuate in Fig. 1a [9], so that we have a deterministic Id-Vg. For nano-scale devices, however, Fig. 1b shows that the current fluctuates, causing uncertainties in the measurement. For example, the Id-Vg triggered from the points 'A' and 'B' in Fig. 1b is given in Fig. 1c and their difference is considerable [9].

It is well-known that nanoscale devices have substantial DDV at time zero after device fabrication, caused by variations in gate work function, line edge roughness, FIN heights, etc [10]. Even if nanoscale devices are identical at time zero, Fig. 2 shows that they become different after ageing [9]. This is because the defect generation during ageing is a stochastic process, resulting in a time-dependent variation (TDV). To characterize TDV, it is essential to repeat tests many times (e.g. 50) on multiple devices. This is costly in test time. For example, if it takes one day to complete the NBTI qualification for large devices, repeating this 50 times will take 50 days.

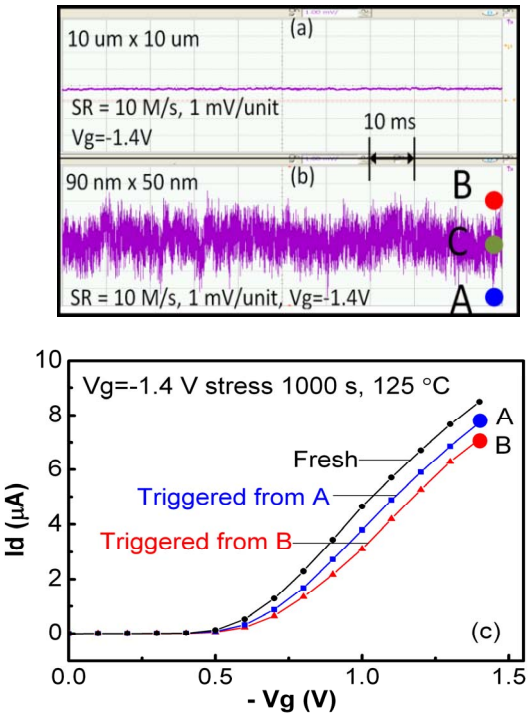

Fig. 1 (a) Drain current fluctuates little in a large device. (b) The fluctuation is considerable in a nanoscale device, causing the measurement uncertainties in (c). The Id-Vg marked by 'A' and 'B' was triggered from the point 'A' and 'B' in (b). A higher value in (b) represents more degradation. [9]

The objective of this work is to review the recent progresses in tackling these challenges, based on the As-grown-Generation (AG) model. Section II describes the Stress-Discharge-Recharge (SDR) technique designed for reliable extraction of the time exponent. Section III introduces the Voltage Step Stress (VSS) as a fast test method to reduce test time and how to combine VSS with SDR. Section IV presents how to overcome the fluctuation-induced measurement uncertainties and how to accelerate the NBTI tests of nanoscale devices by adopting VSS-SDR.

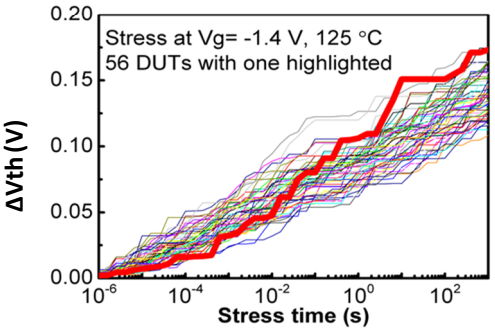

Fig. 2 The ageing induced device-to-device variations. [9]

II. Stress-Discharge-Recharge Technique

Several models have been proposed for NBTI, including the Reaction-Diffusion (RD) framework [4], the Composite model [5], and the As-grown-Generation (AG) model [6-8,11]. All of them can fit the test data well, but AG is the only model that can predict the long term NBTI under use conditions, based on the parameters extracted from accelerated ageing tests [11]. The success of AG model comes from the accurate separation of defects into As-grown defects and Generated defects, as detailed below.

Fig. 3 shows that As-grown defects (AD) have two states: neutral and charged. They are not caused by stress, so that they remain the same before and after stress. Their signatures are shown in Fig. 4 [12]: they can be completely neutralized after charging and the recharge is the same as the first charge. When neutral, their energy levels are below the top edge of Si valence band, Ev, in Fig. 3.

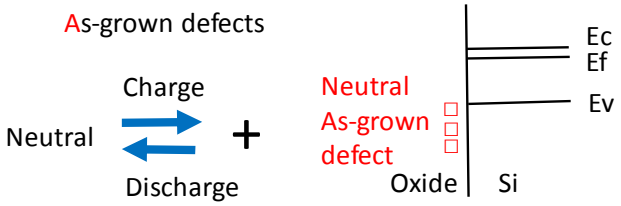

Fig. 3 As-grown defects have two states: neutral and charged. When neutral, they are below Si Ev.

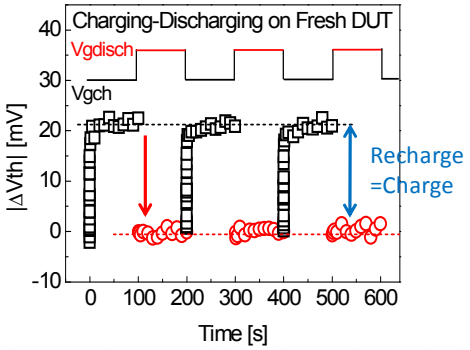

Fig. 4 The signatures of As-grown defects: they can be completely discharged and their recharge is the same as the first charge. [12].

In contrast, Fig. 5 shows that the generated defects have three states: precursor, neutral, and charged. The 'generation' occurs when stress converts precursors to defects. The generated defects (GD) will not return to the precursors without high temperature (~400 °C) annealing [13]. This generation process is slow and follows power law. Once the defects are generated, they can be charged rapidly. These newly generated defects lead to a higher recharge, when compared with the first charge, as shown in Fig. 6 [14].

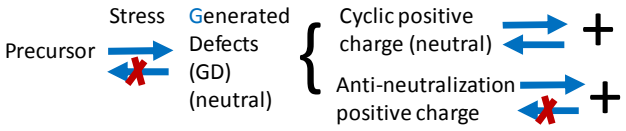

Fig. 5. Generated defects have three states: precursor, neutral, and charged. Once generated, they will not return to precursor during stress. The conversion from precursor to GD follows power law, while charging is a fast process.

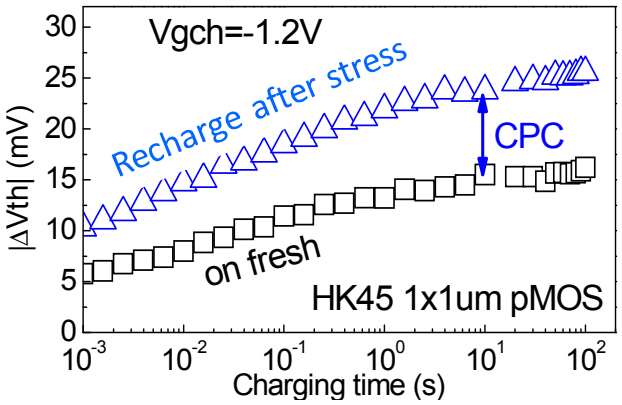

Fig. 6. Generated defects lead to higher charges during recharge after stress-then-discharge, when compared with first charge on a fresh device. [14].

Fig. 7 illustrates that the electron energy level of GD is higher than that of AD. Some charged GDs stay above the Fermi level at the interface, Ef, even during discharge, so that they will not be discharged. They are referred to as Anti-neutralization positive charges (ANPC) [11,15]. Some GDs are below Ef during discharge and can be repeatedly charged-discharged by alternating gate bias polarity. They are called as Cyclic Positive Charges (CPC) [11,15].

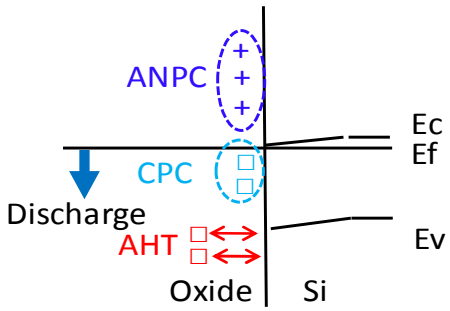

Fig. 7. Generated defects: Anti-neutralization positive charges (ANPC) does not neutralize, while Cyclic positive charges (CPC) does during discharge.

We focus on characterizing the power law generation process in eq.(1) hereafter [6],

$$\Delta V_{th} = C \cdot (V_g - Vth)^m \cdot t^n. \qquad (1)$$

Fig. 8 shows that the extraction of time exponent, n, depends on the measurement conditions, which leads to large errors when the model is used to make prediction by extrapolation. The errors have two sources: inclusion of As-grown defects and the loss of some GDs.

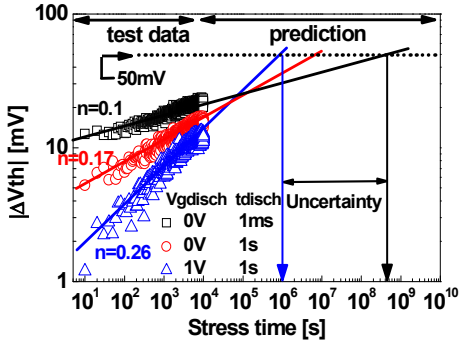

Fig. 8. The extracted time exponent, n, for the GD depends on measurement conditions, leading to large errors when extrapolated to make prediction. [14].

On one hand, as-grown defects are preexisting and they should be excluded from the generation kinetics. If they are included by mistakes, they lead to a smaller extracted 'n' [16]. On the other hand, if the GDs are not captured in their entirety, the loss of GDs will result in a larger 'n' [14].

The Stress-Discharge-Recharge (SDR) technique in Fig. 9 is designed to ensure that ADs are removed and GDs are captured in entirety [14]. During stress, both GDs and ADs are charged. The 'Discharge' step is used to neutralize all ADs, but some GD, i.e. CPC, is also neutralized, as shown in Fig. 7. To regain the lost CPC, a follow-on recharge step is used to recharge the CPC. Fig. 10 shows that the n=0.2 extracted by using SDR is independent of stress and measurement conditions. More details can be found from ref. 14.

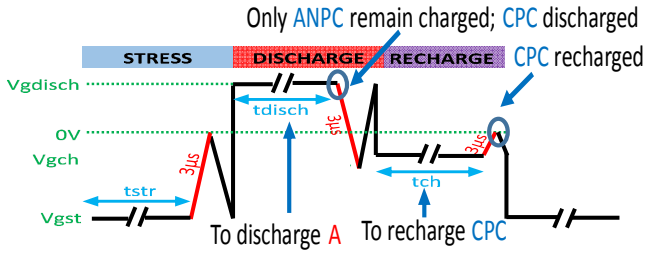

Fig. 9. The Stress-Discharge-Recharge (SDR) technique to remove the As-grown defects and capture all GDs without losses. [14].

III. Voltage Step Stress with SDR

To extract the voltage exponent of the power law kinetics, the standard method is carrying out multiple tests (e.g., 5) under different stress voltages [6]. The stress voltage is kept at constant during each test. These multiple constant voltage stress (CVS) tests are time consuming. To reduce the test time, voltage ramp stress was proposed, where stress bias increases linearly with time [17]. Although this technique can be used to compare the relative NBTI of different processes, Fig. 11 shows that the extracted model cannot be used to make quantitative prediction [18].

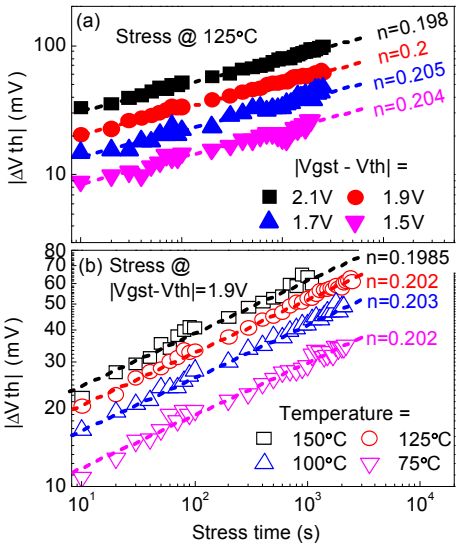

Fig. 10. The n extracted by using Stress-Discharge-Recharge (SDR) technique is independent of stress biases (a) and temperatures (b). [14].

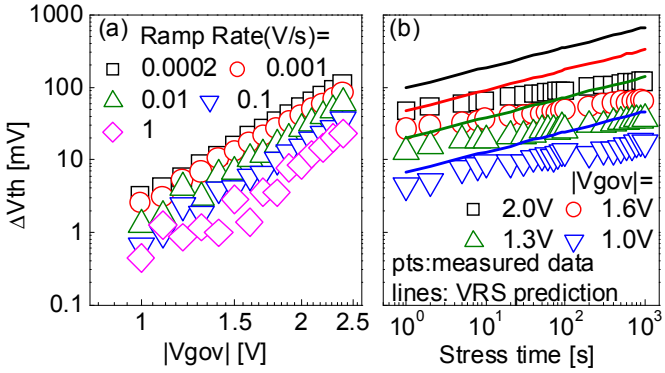

Fig. 11. (a) Test data obtained by the voltage ramp stress under different ramp rates. (b) The lines are the prediction from the model extracted by the voltage ramp stress. The symbols are measured data during the constant voltage stress. The agreement is poor. [18].

To have a fast test technique that can be used to make quantitative prediction, the Voltage Step Stress (VSS) was proposed [16,19]. Here the stress voltage increases in steps and a single VSS test on one device will replace the multiple CVS tests for extracting the voltage exponent, m. As illustrated in Fig. 12, a stress at a higher bias is equivalent to a longer stress time at a lower bias, which can be evaluated by eq.(2) [16,19],

$$t_{eff} = t \cdot \left(\frac{V_2}{V_1}\right)^{\frac{m}{n}}. \qquad (2)$$

The VSS technique can be combined with SDR method as shown in Fig. 13. A device is stressed for 10 sec at each voltage

step, which is long enough to fill the as-grown hole traps to saturation [6]. This is followed by a discharge period of 10 sec and a recharge of 10 sec. The test time is 30 sec for each step. If one uses a voltage step size of 20 mV, 100 steps will cover a range of 2 V and the total time is only 3,000 sec.

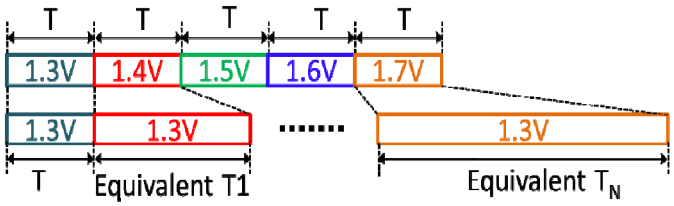

Fig. 12. A schematic illustration of the Voltage Step Stress (VSS) technique. The stress bias increases in steps and the stress under higher bias is equivalent to the stress under lower bias for a longer time. [16].

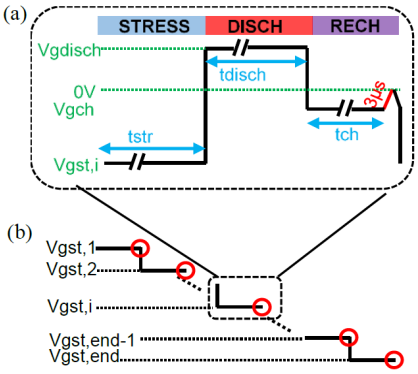

Fig. 13. A combination of voltage step stress with stress-discharge-recharge method (VSS-SDR). [18].

A typical result is given in Fig. 14a. When the stress overdrive voltage |Vgov| is low, ΔVth is a constant after recharging at Vg=-1.2 V. This is because the defect generated in 10 sec stress under low stress |Vgov| is negligible, so that the flat ΔVth originated from filling the as-grown defects, which are not affected by stresses. As stress |Vgov| increases, the increased GD leads to a gradual rise of ΔVth. The GD can be evaluated by subtracting the flat level, as shown in Fig. 14a.

| The voltage exponent, m, can be extracted from the GD data obtained from a single VSS-SDR test by using eq.(2), which converts the GD at a higher bias to a longer stress at a lower bias. On one hand, if the used m is too high (e.g. m=7), Fig. 14b shows that the effective stress time is too long. When the converted data is used to fit a power law, the fitted n will be lower (e.g. n=0.125) than the n=0.2 determined in section II. On the other hand, if the used m is too low (e.g. m=2), teff is too short, so that the fitted n will be higher (e.g. n=0.33). The correct m will give the predetermined n=0.2. For the example in Fig. 14, m=4.28 is extracted.

To verify the model parameters extracted from the fast VSS-SDR technique for GD, they are used to predict the GD under CVS and compared with the GD measured under CVS. Fig. 15 shows that the agreement is good.

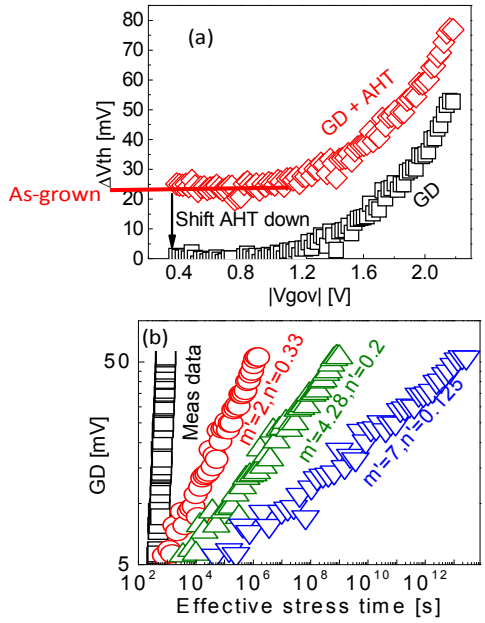

Fig. 14. (a) An example of the VSS-SDR with a voltage step of 20 mV. Each point corresponds to one voltage step. (b) Extraction of voltage exponent, m. The correct m gives the same fitted 'n=0.2', as that extracted in Fig. 10. [18].

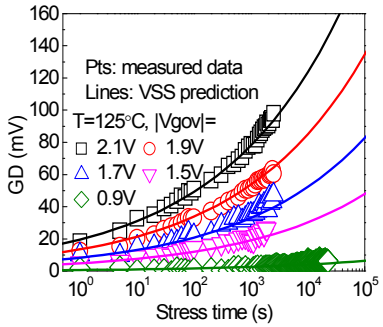

Fig. 15. A comparison of the prediction with the test data. The lines are the prediction of the models extracted from the fast VSS-SDR techniques. The symbols were test results under constant voltage stresses. [18].

IV. Application of VSS-SDR on nanoscale devices

As shown in Figs. 1b&c, the fluctuation in drain current causes considerable uncertainties in the measurement of nanoscale devices. To address this fluctuation, the pulse Id-Vg was repeated 100 times after each stress step and the statistical distribution of the 100 measurements is given in Fig. 16a. Higher stress biases result in higher average ΔVth, but the parallel shift of the distribution suggests the statistical variation remains the same. This is confirmed by the insensitive of the standard deviation to the stress voltage in Fig. 16b.

To understand this insensitivity to the stress Vgov, it should be pointed out that the fluctuation is dominated by the traps near to Ef, whose occupancy changes readily. When a pMOSFET is switched on, Ef at the interface is close to Ev, where as-grown hole traps (AHT) are located. Since AHTs do not change by stress, the AHT-induced fluctuations do not change, either.

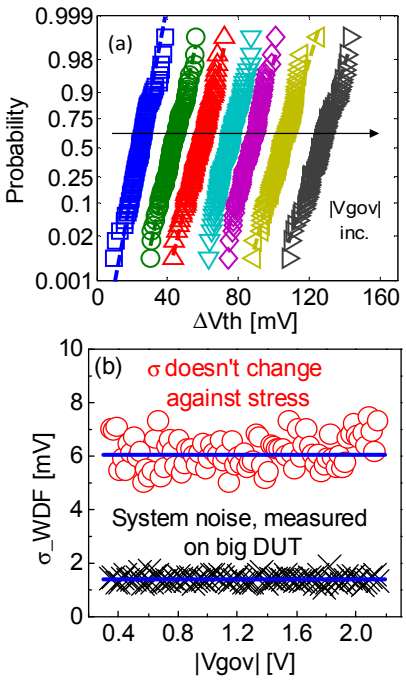

Fig. 16. (a) The statistical distribution of ΔVth when measured 100 times by pulse Id-Vg after each voltage step stress. (b) The standard deviation. [18].

The uncertainties in measurement can be overcome by using the average value of the 100 pulse Id-Vg. In Fig. 17, the grey lines are the 100 ΔVth measured at each Vgov and the symbol '◊' is their average value. Like the large device in Fig. 14a, there is a flat region at low |Vgov|, where As-grown defects dominates and GD is negligible. The GD can be obtained by subtracting this flat level. This removes the impact of fluctuation on GD measurement. Some abrupt increase in GD can be observed, originating from the generation of a dominant trap.

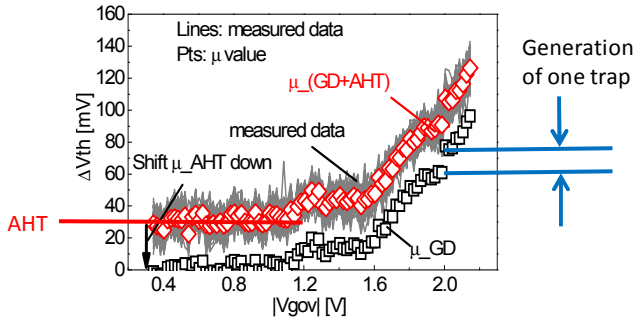

Fig. 17. A typical VSS-SDR result of nanoscale devices. The grey lines represent the 100 data at each Vgov and '◊' is their average. The GD ('□') is obtained by subtracting the AHT. [18].

To characterize the GD-induced device-to-device variation (DDV), the VSS-SDR was repeated on multiple devices. In Fig. 18a, each grey line represents the GD in Fig. 17 for one device and the symbols are the mean value of multiple devices. It can be seen that the mean GD of 25 devices is as well behaved as that of a large device in Fig. 14a, so that it can be analyzed accordingly in Fig. 18b. Since each VSS-SDR test takes less than one hour, the characterization of GD-induced DDV can be completed in one day.

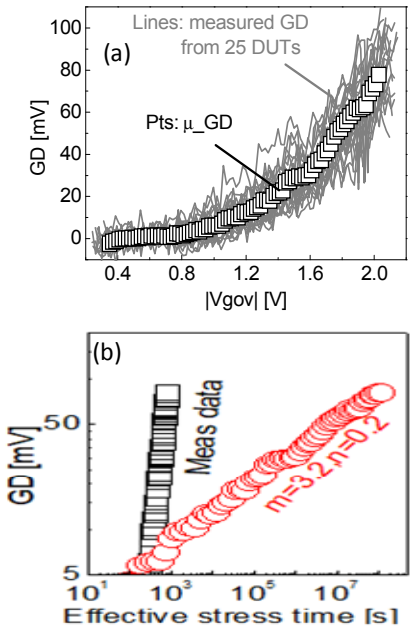

Fig. 18. (a) The GD of multiple devices. Each grey line represents one device and the symbols are the mean values. (b) Extraction of voltage exponent, m from the mean GD. [18].

The statistical distribution of GD under different Vgov is plotted in Fig. 19a. Fig. 19b shows that its standard deviation follows a power law with an exponent of 0.5. This agrees well with the defect-centric model, where the number of traps per device follows a Poisson distribution and the ΔVth induced by one trap follows an exponential distribution [18,20].

Finally, the model extracted from VSS-SDR is used to predict the GD of nanoscale devices under constant voltage stresses. Fig. 20 shows a good agreement and details can be found from ref. 18.

IV. Conclusion

Based on the As-grown-Generation (AG) model, this paper addresses the challenges for characterizing the NBTI generated defects in nanoscale devices: measurement uncertainties induced by within-a-device-fluctuation and the long test time to capture the device-to-device variation. The method requires the time exponent, n, being reliably determined and independent of stress and measurement conditions. This is achieved by using the Stress-Discharge-Recharge (SDR) technique. To reduce the test time, the SDR is combined with the fast voltage step stress (VSS), which replaces multiple constant voltage stresses by a single test. After verifying the accuracy of VSS-SDR on large devices, its applicability to nanoscale devices is demonstrated. The uncertainties are overcome by using the average value of multiple Id-Vg measurements. This fast VSS-SDR technique allows characterizing the DDV of GD in one day. The distribution of DDV agrees with the defect-centric model.

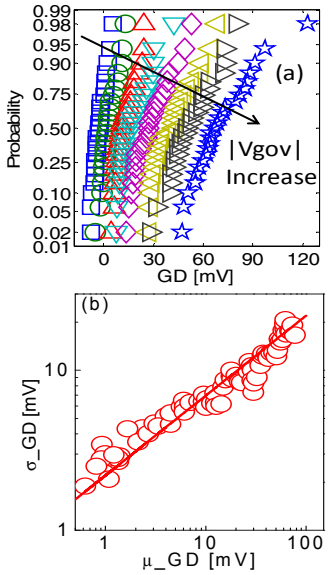

Fig. 19. (a) The statistical DDV of GD under different Vgov. (b) Its standard deviation against mean value. The line is fitted with an exponent of 0.5. [18].

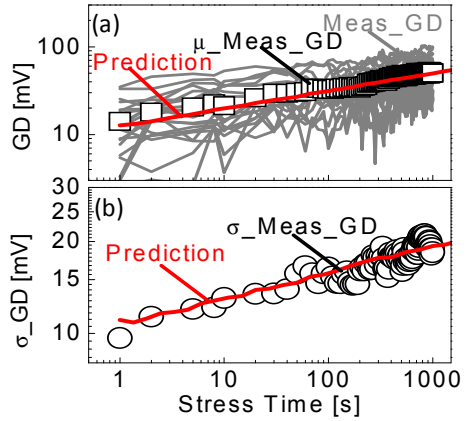

Fig. 20. (a) Each grey line is the GD of one device under constant voltage stress. '□' is the mean value. The red line is the prediction of the model extracted from the fast VSS-SDR tests. (b) The standard deviation of the data in (a). [18].

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