Evaluation of DC-link Voltage Ripple in Seven-Phase PWM Voltage Source Inverters

Marija Vujacic
Dept. of Electrical, Electronic and Information Engineering
Alma Mater Studiorum University of Bologna
40136 Bologna, Italy
Email: marija.vujacic2@unibo.it

Obrad Djordjevic
Dept. of Electronics and Electrical Engineering,
Liverpool John Moores University
Livetpool, UK
Email: O.Dordevic@ljmu.ac.uk

Gabriele Grandi
Dept. of Electrical, Electronic and Information Engineering
Alma Mater Studiorum University of Bologna
40136 Bologna, Italy
Email: gabriele.grandi@unibo.it

***Abstract*— The analysis of dc-link inverter current and voltage ripple is important for the optimization of the input components, mainly the dc-link capacitor. In this paper reference is made to two-level seven-phase PWM voltage source inverters with balanced load, typically multiphase ac motors. The peak-to-peak amplitude of the dc-link voltage switching ripple within the fundamental period is analytically determined as a function of operating conditions: modulation index, output currents amplitude and phase angle. The maximum of voltage switching ripple is also derived in order to design the dc-link capacitor. The two most popular inverter modulation techniques are considered: sinusoidal PWM and centered PWM (CPWM, equivalent to space vector modulation, SVM). A comparison between them is made in terms of the dc voltage switching ripple envelope. Numerical simulations are carried out by Matlab/Simulink in order to verify the analytical results.**

Keywords— voltage source inverters; seven-phase systems; dc-bus voltage ripple, dc-link capacitor.

I. INTRODUCTION

Dc-link capacitor is an important part of power converters since it serves to balance the instantaneous power difference between the dc source and the output load, as well as to reduce the emission of electromagnetic interference and limit voltage ripple both for steady-state and transient. Depending on the wide range of power electronic applications, such as photovoltaic systems, wind turbines, industry motor drives, automotive etc., different types of capacitors are manufactured. Fundamental and widely used are: Aluminum electrolytic capacitors, film capacitors and ceramic capacitors [1]. They are used in both low and high power applications covering the wide range of size, voltage and capacitance variations.

Conventional designs have been using the set of aluminum electrolytic capacitors due to their large capacitance per unit volume. However, the dc link current and voltage study [2] shows that a single low-inductance high-current film capacitor could be used instead. It results in size reduction, reliability improvement and significant voltage spike reduction. In addition, the electrolytic capacitor has limited life expectancy because its electrolyte tends to dry out with time. Substituting the film capacitor allows the life expectancy to be extended. Although, film capacitors do cost more per uF comparing to electrolytic ones, it is shown in [3] that needed amount of the dc-link capacitance is much less for a film capacitor than an electrolytic capacitor. The reason is that a film capacitor is not limited by ripple current rating but rather by the maximum dc-link voltage ripple. The dc-link capacitor design based on the maximum dc-link voltage ripple is proposed in [4] for single-phase H-bridge inverter. Both, low- and switching-frequency voltage ripple components are considered and simple equations for calculating the dc-link capacitance are obtained. Similarly, the peak-to-peak dc-link voltage switching ripple envelope is defined in [5] for three-phase inverters. The maximum value of the voltage ripple is determined as a function of modulation index for different output phase angles. Simple formulas for dc-link capacitor design and selection are proposed basing on it. Further extension of the analysis to multiphase inverter topologies, in particular five-phase case, has been given by [6].

The frequency spectrum of the dc-link capacitor current ripple in electric vehicle inverter systems has been investigated in [7] for three commonly used modulation strategies - sinusoidal pulse width modulation (SPWM), space vector modulation (SVM) and third-harmonic injection (THI). Two design schemes using electrolytic and film capacitors are compared through simulation and experiments in terms of power loss, core temperature, capacitor life-time and battery current harmonics. The comparison shows that the film capacitor application has significant advantages in terms of improved power density, low power loss, low parasitic inductance, and long lifetime.

Regarding the dc-link current and voltage analysis in multiphase inverters, most of the analysis are related to the RMS calculations of the input (dc-link) current. Namely, the impact of PWM modulation on the RMS value of input current ripple has been studied for five-phase inverters in [8] and for dual three-phase induction machine in [9]. It has been shown in [10] that PWM strategies have different effect on the RMS of the input current and on the quality of the output current. Hence, both constraints have to be taken into account for the dc-link capacitor sizing. The RMS calculations of input current ripple in five-, six- and nine- phase systems are reported in [11]-[13], respectively. Based on the reviewed literature, there are no available papers dealing with the analysis of the dc-link voltage ripple in seven-phase inverters. The seven-phase configuration is poorly discussed only in terms of comparison of the input current ripple within different multiphase inverter topologies in [14] and [15].

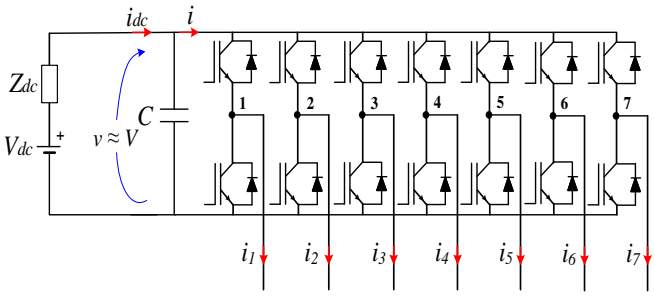

Fig. 1. Circuit scheme of the considered seven-phase VSI.

In this paper, the analysis of input current and voltage ripple in seven-phase PWM voltage source inverters with balanced load (Fig. 1), typically multiphase ac motors, is presented. The reference is made to both commonly used modulation techniques: sinusoidal PWM (SPWM) and centered PWM modulation (CPWM, equivalent to space vector modulation). The peak-to-peak dc voltage ripple amplitude is analytically determined over the fundamental period as a function of operational conditions (the modulation index and the phase angle of the output current). Further, maximum of the peak-to-peak voltage ripple amplitude is determined as a function of modulation index and different diagrams are presented covering the full range of output phase angles. The comparison between modulation techniques is made in terms of the dc-link voltage ripple amplitude. Based on the analysis of the dc-link components, simple guidelines for calculating the dc-link capacitance are proposed. The simulations are carried out by Matlab/Simulink to verify proposed theoretical developments. A good matching is achieved for all the cases.

II. System configuration and DC current analysis

A. System configuration

Fig. 1 shows the analyzed circuit topology, two-level seven-phase PWM VSI. By neglecting the dc-link voltage oscillations ($v \cong V$ = const), and by considering only linear modulation range, the desired inverter phase voltages are sinusoidal and symmetrical, expressed as:

$$v_k^* = mV\cos\left(\vartheta-(k-1)\frac{2\pi}{7}\right),\ k=1,2,\ldots,7 \quad (1)$$

where $\vartheta=\omega t$, $\omega=2\pi/T$ and T is the fundamental period. The modulation index m is defined as a ratio between the amplitude of the desired phase voltage V_0 and V, i.e. $m=V_0/V$.

Considering sinusoidal PWM output voltages given by (1), for balanced load and neglecting the output current ripple, the corresponding seven-phase output currents are assumed sinusoidal and symmetrical as well:

$$i_k = I_0\cos\left(\vartheta-(k-1)\frac{2\pi}{7}-\varphi\right),k=1,\ 2,\ \ldots,7 \quad (2)$$

where I_o is the output current amplitude and φ is the phase angle.

B. DC current components

Generally, the dc current $i(t)$ can be decomposed into three components: the average component $I = I_{dc}$, the low-frequency component, and the high-frequency (switching frequency) component $\Delta i(t)$. Since the load is balanced in the considered case, the low-frequency component is zero. Consequently, the dc current only contains the average and the high frequency component, according to:

$$i = I_{dc} + \Delta i(t)\,. \quad (3)$$

Under the assumption of ideal power switches, the dc current averaged over the switching period T_{sw}, can be obtained from the input/output power balance, considering the load power angle φ. Therefore, the averaged dc current is given by:

$$I_{dc} = \frac{7}{2}mI_0\cos\varphi\,. \quad (4)$$

The dc current i is the sum of seven inverter leg currents. Each inverter leg current can be calculated from the binary switching function S_k = [0,1], k = 1,2,..,7 (where 0 implies that upper switch is OFF, and 1 implies that upper switch is ON), and corresponding output current. Consequently, the dc current can be expressed as:

$$i = S_1i_1 + S_2i_2 + S_3i_3 + S_4i_4 + S_5i_5 + S_6i_6 + S_7i_7\,. \quad (5)$$

The switching frequency current component can be finally calculated utilizing equations (3)-(5) as:

$$\Delta i(t) = i - I_{dc} = \\ = \left(S_1i_1+S_2i_2+S_3i_3+S_4i_4+S_5i_5+S_6i_6+S_7i_7\right)-\frac{7}{2}mI_o\cos\varphi \quad (6)$$

Due to the symmetry of the dc current waveforms, the following analysis can be limited to one fourteenth of the fundamental period (T/14), i.e. first π/7 radians.

C. PWM modulation fundamentals

Two commonly used modulation techniques are considered for the dc-link voltage ripple evaluation. Therefore, sinusoidal PWM (SPWM) and continues symmetric centered PWM (CPWM, equivalent to space vector modulation) are briefly reviewed.

In general, seven-phase reference signals are obtained using seven fundamental sinusoidal signals (1), which are summed with an appropriate common-mode injected signal v_i and expressed as:

$$v_k^* = mV\cos\left(\vartheta-(k-1)\frac{2\pi}{7}\right)+v_i,\ k=1,2,\ldots 7. \quad (7)$$

In case of SPWM the injected signal is equal to 0. Consequently, the reference signals correspond to sinusoidal voltages given by (1).

In case of CPWM (equivalent to SVM), the centering process is called "min-max" injection, assuming the form:

$$v_i = -\frac{1}{2}\left(v_{\max}+v_{\min}\right), \quad (8)$$

where $v_{\max}=\max\left[v_1^*,v_2^*,...,v_n^*\right]$ and $v_{\min}=\min\left[v_1^*,v_2^*,...,v_n^*\right]$.

Since the timing waveforms of both modulations have the same pattern in Sector I of SVM and/or the first π/7 radians, the following evaluation will be reduced to that range. From the mutual order of the reference signals in the first sector, the following application times t_k can be derived for both SPWM and SVM [16]:

$$t_0 = \frac{T_{sw}}{2}(1/2-m\cos(\vartheta))\,, \quad (9)$$

$$t_1 = mT_{sw}\sin(\pi/7)\sin(\pi/7-\vartheta)\,, \quad (10)$$

$$t_2 = mT_{sw}\sin(5\pi/7)\sin(\vartheta)\,, \quad (11)$$

$$t_3 = mT_{sw}\sin(3\pi/7)\sin(\pi/7-\vartheta)\,, \quad (12)$$

$$t_4 = mT_{sw}\sin(3\pi/7)\sin(\vartheta)\,, \quad (13)$$

$$t_5 = mT_{sw}\sin(5\pi/7)\sin(\pi/7-\vartheta)\,, \quad (14)$$

$$t_6 = mT_{sw}\sin(\pi/7)\sin(\vartheta)\,, \quad (15)$$

$$t_7 = \frac{T_{sw}}{2}(1/2 - m\cos(\pi/7 - \vartheta)). \quad (16)$$

The application times (10)-(15) are identical for SPWM and SVM. The exception is the time sharing of the null configuration between the application times of the two redundant switching states. In case of so called "centered modulation" (CPWM, equivalent to SVM) the total application time of the zero state (t_0+t_7) is equally distributed among two zero space vectors ($t_0 = t_7$).

$$t_0 = t_7 = \frac{T_{sw}}{2} - (t_1 + t_2 + t_3 + t_4 + t_5 + t_6) = \\ = \frac{T_{sw}}{2}\left[\begin{matrix}1 - 2m\left(\sin(\pi/7) + \sin(3\pi/7) + \sin(5\pi/7)\right) \\ \left(\sin(\pi/7)\cos(\vartheta) + \left(1 - \cos(\pi/7)\sin(\vartheta)\right)\right)\end{matrix}\right]. \quad (17)$$

III. DC-LINK VOLTAGE RIPPLE EVALUATION

A. DC-link voltage components

The instantaneous dc-link voltage components can be calculated on the basis of the dc current components. Hence, similarly to the inverter dc current, the dc-link voltage can be decomposed into three corresponding components. Due to the previous consideration of the balanced load conditions, the low-frequency component is zero. Then, the instantaneous dc-link voltage can be given by the (dc) average and the switching voltage components:

$$v(t) = V + \Delta v(t). \quad (18)$$

The evaluation of the switching frequency dc-link voltage component Δv can be done on the basis of the switching frequency dc current component Δi, under the assumption that the reactance of the dc-link capacitor $1/(2\pi f_{sw}C)$ is much smaller comparing to the equivalent dc source impedance Z_{dc} calculated at the switching frequency (f_{sw}=$1/T_{sw}$).

The peak-to-peak amplitude Δv_{pp} of the switching frequency dc-link voltage component Δv can be defined as the difference between its maximum and minimum value within a switching period:

$$\Delta v_{pp} = \max\{\Delta v(t)\}_{T_{sw}} - \min\{\Delta v(t)\}_{T_{sw}}. \quad (19)$$

Due to the symmetry among the seven phases in the considered case of sinusoidal balanced output currents, only the first phase is examined in the following analysis.

B. Peak-to-peak voltage ripple evaluation

The voltage excursion can be calculated within each application time interval t_k based on the equation for the voltage drop over capacitor as:

$$\Delta v_{pp}^{k} = \frac{1}{C}\Delta i\ t_k. \quad (20)$$

Within the considered interval, Δi is assumed to be constant. Finally, the global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by combining different application intervals and finding the maximum within the switching period, as shown in the following.

In Fig. 2 the peak-to-peak dc-link voltage variation Δv_{pp} and the instantaneous input current $i(t)$ (blue staircase line) are shown in one switching period. Within the first sector, if CPWM is applied and depending on the value of I_{dc}, six different cases can be distinguished. Hence, the corresponding peak-to-peak dc-link voltage variations can be calculated as:

- case A: when $i_1 \geq I_{dc}$,

$$\Delta v_{pp}^{A} = \frac{1}{C} I_{dc} 2t_0. \quad (21)$$

- case B: when $i_1 \leq I_{dc} < i_1+i_2$,

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + \frac{1}{C}(I_{dc} - i_1) 2t_1. \quad (22)$$

- case C: when $i_1+i_2 \leq I_{dc} < i_1+i_2+i_7$,

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + \frac{1}{C}(I_{dc} - i_1 - i_2) 2t_2. \quad (23)$$

- case D: when $i_1+i_2+i_7 \leq I_{dc} < -(i_4+i_5+i_6)$,

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + \frac{1}{C}(I_{dc} - i_1 - i_2 - i_7) 2t_3. \quad (24)$$

- case E: when $-(i_4+i_5+i_6) \leq I_{dc} < -(i_4+i_5)$,

$$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + \frac{1}{C}(I_{dc} + i_4 + i_5 + i_6) 2t_4. \quad (25)$$

- case F: when $-(i_4+i_5) \leq I_{dc} < -i_5$,

$$\Delta v_{pp}^{F} = \Delta v_{pp}^{E} + \frac{1}{C}(I_{dc} + i_4 + i_5) 2t_5. \quad (26)$$

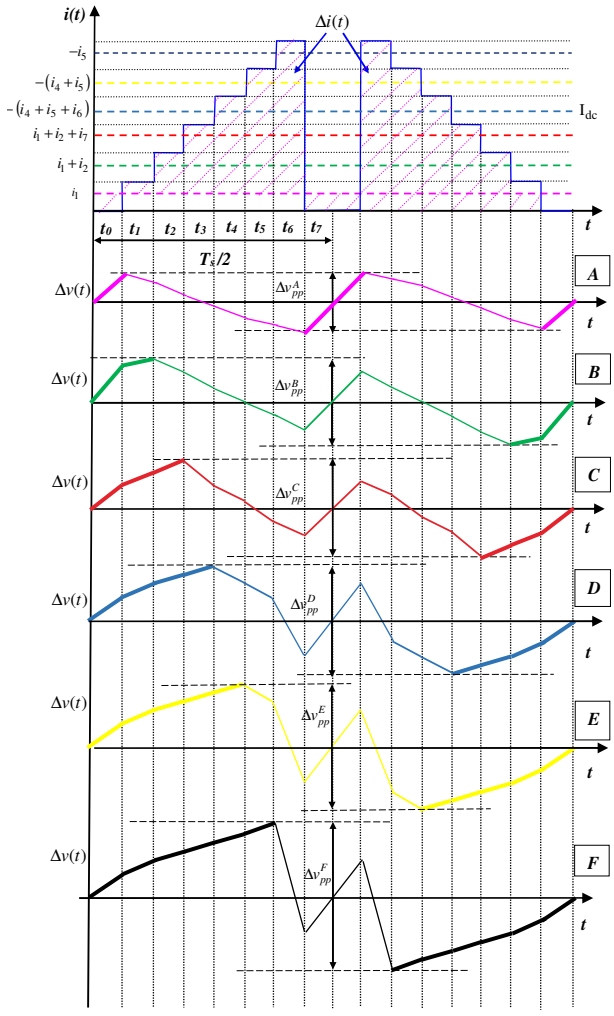

Fig. 2. Dc-link current and voltage ripple in one switching period T_{sw}, for seven-phase VSIs.

When sinusoidal PWM is applied there is an additional case

- case G: when $i_1 \geq I_{dc}$, since $t_o \neq t_7$,

$$\Delta v_{pp}^{G} = \frac{1}{C} I_{dc} 2t_7. \tag{27}$$

For final calculations, the application times (9)-(17), as well as the currents given by (2), (4), and (6), should be used. The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by finding the maximum value of possible six (SVM) or seven (SPWM) cases, i.e. Δv_{pp}=max (Δv_{pp}^{A},…, Δv_{pp}^{G}).

In order to emphasize the influence of the modulation strategy, the dc-link peak-to-peak voltage ripple amplitude can be normalized introducing r_{pp}, according to:

$$\Delta v_{pp} = \frac{I_o}{f_{sw} C} r_{pp}(m, \vartheta, \varphi). \tag{28}$$

Normalized peak-to-peak voltage ripple amplitudes r_{pp}^{SVM} and r_{pp}^{SPWM}, can be defined by (28) with reference to SVM and SPWM, respectively.

C. Peak-to-peak ripple diagrams

In order to predict the behavior of the dc voltage ripple, Fig. 3 shows normalized functions of the dc voltage ripple amplitude, over a fundamental period ϑ = [0, π/7], for three values of modulation index (1/4, 1/3 and 1/2) and four output phase angles (φ = 0 °, 30 °, 60 °, and 90°). The results are shown with reference to both SPWM and SVM (solid and dashed lines, respectively).

It can be noted that normalized voltage ripple amplitude $r_{pp}(\vartheta)$ has a higher value corresponding to lower load phase angle, actually the highest value for the unity power factor (φ = 0°) where $r_{pp}^{max}(\vartheta) \cong 0.25$. The same behavior of the dc voltage ripple has been noticed in case of five-phase inverters in [6]. On the other side, comparing to the three-phase case investigated in [5], it becomes obvious that by increasing the number of phases the profile of the voltage ripple amplitude becomes more flat. Wider excursion of the voltage ripple amplitude in the three-phase case is observed for all considered cases of modulation index and output phase angle, unlike the five- and seven-phase cases. Still, for all three mentioned topologies the voltage ripple amplitude is generally ranging between 0 and 0.25. It is of importance to mention here that for the fair comparison of the different inverter topologies, the same output power (or the same total output current) should be considered. Therefore, it brings to a conclusion that the dc-link voltage ripple amplitude is reduced by increasing the number of phases, especially from three to five and less significant, but still noticeable, increasing the number of phases from five to seven. This is an important point for the dc-link capacitor design and its proper sizing in multiphase voltage source inverters.

In addition, referring to the two applied modulation techniques and observing Fig. 3, no significant influence on the voltage ripple amplitude has been shown. Only for the highest considered modulation index value (m=1/2) a slight reduction is achieved as a consequence of SPWM.

As mentioned before, for the dc-link capacitor design, it is of importance to know the maximum (peak-to-peak) value of the voltage ripple. Hence, the maximum ripple amplitude is depicted in Fig. 4 as a function of modulation index. Again, four output phase angles are considered in order to cover full range of operational conditions.

IV. DC-LINK CAPACITOR DESIGN

In this sub-section, simple guideline for designing the dc-link capacitor is proposed on the basis of the maximum peak-to-peak voltage ripple value shown in Fig. 4. Namely, when the switching frequency is high enough (i.e. in the order of kHz), the amplitude of the dc voltage ripple is determined only by the size of the dc-link capacitor.

Observing Fig. 4 and setting $r_{pp}^{\max}$ in (28) to the appropriate value, the dc-link capacitance can be easily calculated from a simple formula given by

$$C = r_{pp}^{\max} \frac{I_o}{f_{sw} v_{pp}^{req}}, \tag{31}$$

where v_{pp}^{req} is the required dc-link voltage ripple value.

In the following, two extreme cases (φ = 0° and φ = 90°) are analyzed and the dc-link capacitance is calculated accordingly.

Firstly, it can be noted that the maximum peak-to-peak voltage ripple amplitude $r_{pp}^{\max}$ has the highest value for the unity power factor (φ = 0°) and it is equal to:

$$r_{pp}^{\max} \cong 0.25 = \frac{1}{4}. \tag{32}$$

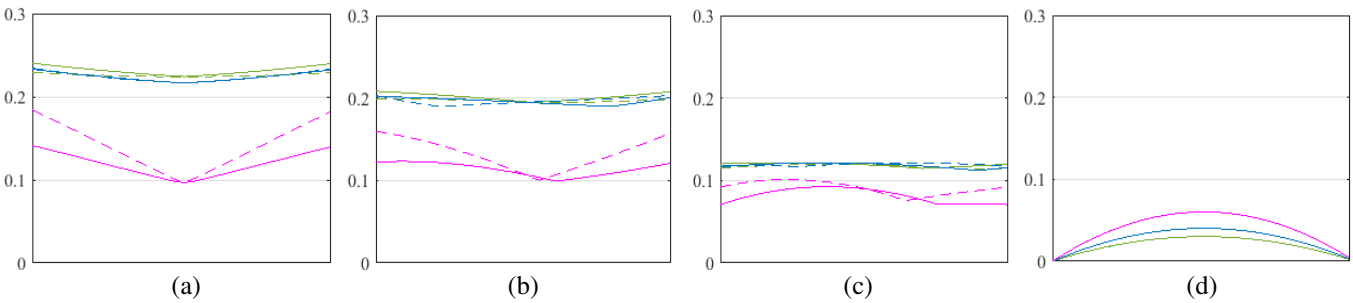

Fig.3. Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over the period [0, π/7] for different modulation indices, m = 1/4 (green), 1/3 (blue), and 1/2 (pink), and output phase angles a) φ = 0°, b) φ = 30°, c) φ = 60° and d) φ = 90°.

Introducing (32) in (31), the dc-link capacitance is calculated as:

$$C = \frac{1}{4}\frac{I_o}{f_{sw} v_{pp}^{req}}. \quad (33)$$

In case of φ = 90°, $r_{pp}^{\max}$ is directly proportional to the value of modulation index *m*. It is clear form Fig. 4 that the dc-link capacitor would be oversized if the design is based on (33). Of course, the maximum value of modulation index should be considered, leading to the following simplification:

$$r_{pp}^{\max} = 0.06 \cong \frac{1}{17}. \quad (34)$$

As in (33), by specifying v_{pp}^{req}, the dc-link capacitance can be calculated utilizing (31) and (34) as

$$C = \frac{1}{17}\frac{I_o}{f_{sw} v_{pp}^{req}}. \quad (35)$$

The same procedure can be followed for any specific value of modulation index and phase angle, by simply finding the corresponding maximum peak-to-peak voltage ripple amplitude $r_{pp}^{\max}$ (Fig. 4) and by replacing it in (31).

V. Numerical Simulations

The proposed theoretical analysis is validated using Matlab/Simulink. The parameters of the simulated seven-phase system are given in Table I. The obtained results are shown in Fig. 5 and Fig. 6 for SPWM and CPWM, respectively.

The dc-link voltage switching ripple (blue trace) is shown together with the corresponding envelopes (red traces). The switching voltage ripple is obtained by simply subtracting the dc average voltage component from the dc supply voltage basing on (18). The envelopes are calculated as one half of the peak-to-peak voltage ripple value. Two output phase angles φ = 30° (a) and φ = 60° (b) are considered, representing e.g. common induction motor loaded at 75% and 25%, respectively. Two values of modulation index m=0.25 (upper) and m= 0.5 (lower) are shown as well.

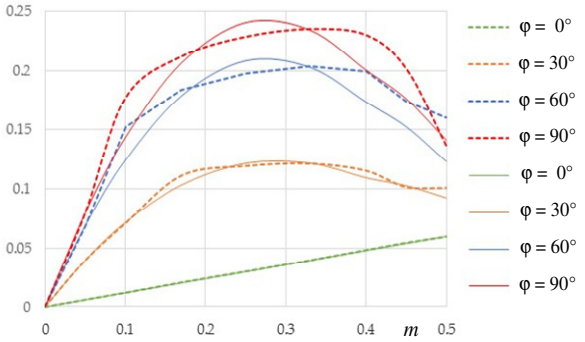

Fig. 4. Maximum of normalized peak-to-peak voltage ripple amplitude vs. modulation index for different output phase angles and two modulations (SPWM – bold traces, CPWM – dashed traces).

There is a good agreement between the dc voltage ripple and the calculated envelopes, in terms of both - the absolute amplitude and the shape, for all considered cases and over the whole fundamental period.

TABLE I: Simulation Circuit Parameters

Label	Description	Parameters
V_{dc}	DC voltage supply	300 V
R_{dc}	DC source resistance	5.3 Ω
L_{dc}	DC source inductance	4.5 mH
C	DC-link capacitance	200μF
f	Fundamental frequency	50 Hz
f_{sw}	Switching frequency	2 kHz
I_o	Output currents amplitude	1 A

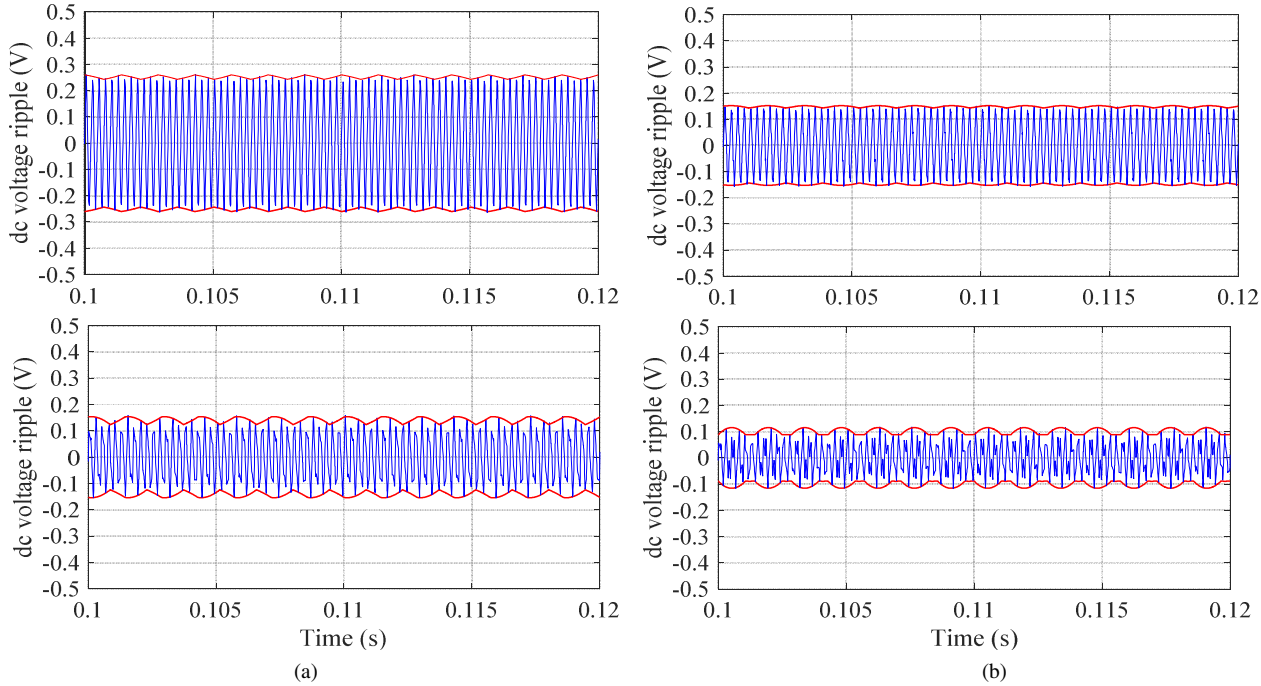

Fig. 5. Dc-link voltage ripple (v_{pp}): simulation results (blue trace) and calculated peak-to-peak envelope (red trace) in case of SPWM for φ = 30° (a) and φ = 60° (b), *m* = 0.25 (upper) and *m* = 0.5 (lower).

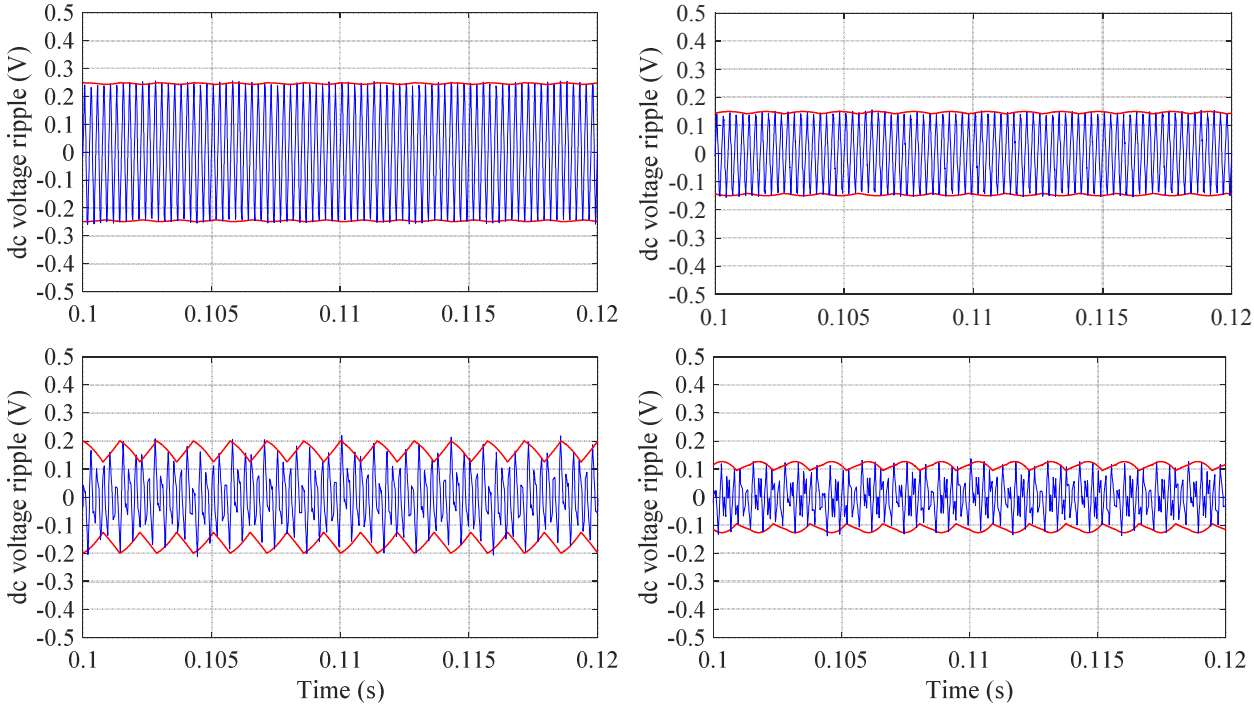

Fig. 6. Dc-link voltage ripple (v_{pp}): simulation results (blue trace) and calculated peak-to-peak envelope (red trace) in case of CPWM for φ = 30° (a) and φ = 60° (b), m = 0.25 (upper) and m = 0.5 (lower).

VI. Conclusion

In this paper, the peak-to-peak amplitude of dc-link voltage ripple in seven-phase VSIs with balanced load is analytically determined. In particular, dc-link current and voltage ripple are analyzed, and the amplitude of the voltage switching ripple is analytically derived as a function of operating conditions. The normalized peak-to-peak voltage ripple amplitude is introduced in order to emphasize the influence of applied modulation techniques and to determine the ripple profile over the fundamental period as well. Different operatig conditions (modulation indices and output phase angles) are presented. No significant influence of the applied modulation techniques is observed, except for high values of modulation index when sinusoidal PWM is preferred to centered PWM since it leads to the lower voltage ripple amplitudes. Maximum of voltage switching ripple within the fundamental period is also derived in order to design the dc-link capacitor. Numerical simulations confirmed the theoretical analysis, always showing a good matching between the actual dc voltage switching ripple and the theoretical envelope.

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